

QFN PCB Design Guidance Notes

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General guidelines on using the CML QFN package

QFN PCB Design Guidance Notes

1. Introduction

QFNs are near chip scale plastic encapsulated leadless packages that CML has adopted for a number of its designs. The package uses a conventional copper lead-frame based technology and is a cost effective solution where board space economy is an issue. There are benefits of improved electrical and thermal performance over the more traditional leaded packages.

2. QFN Typical Package Cross-Section

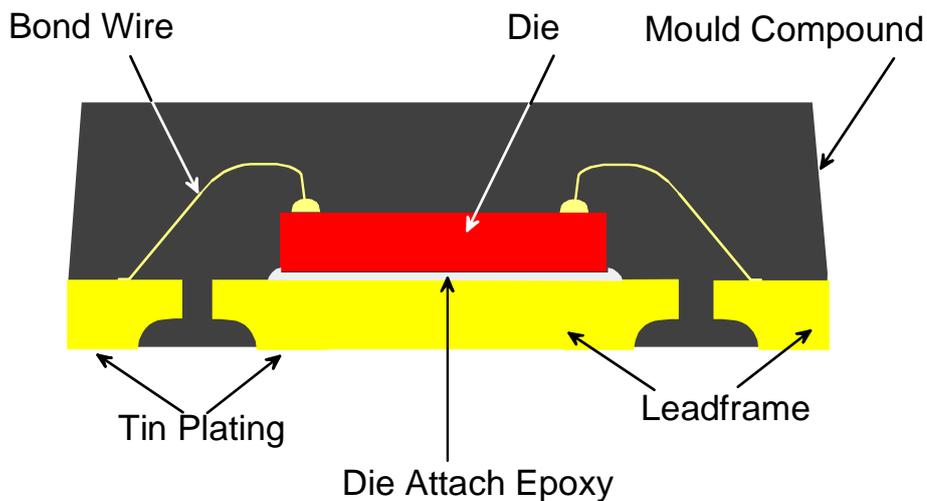


Figure 1

3. VQFN Packages currently used by CML

All packages conform to JEDEC outline MO-220. CML may use multiple suppliers of QFNs and some variations in package may be noticeable under visual inspection. Any differences are purely cosmetic. There is no difference in mechanical strength and reliability. Solder fillets up the side of the QFN package are not required for acceptability of soldering (see IPC A-610).

CML Part No	Size	Lead Count	Lead Pitch
Q1	9mm x 9mm	64	0.5 mm
Q2	8mm x 8mm	56	0.5 mm
Q3	7mm x 7mm	48	0.5 mm
Q4	6mm x 6mm	40	0.5 mm
Q5	5mm x 5mm	32	0.5 mm
Q6	4mm x 4mm	24	0.5 mm
Q7	4mm x 4mm	16	0.5 mm
Q8	5mm x 5mm	28	0.5 mm
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Table 1

4. Schematic of the Underside of a typical QFN

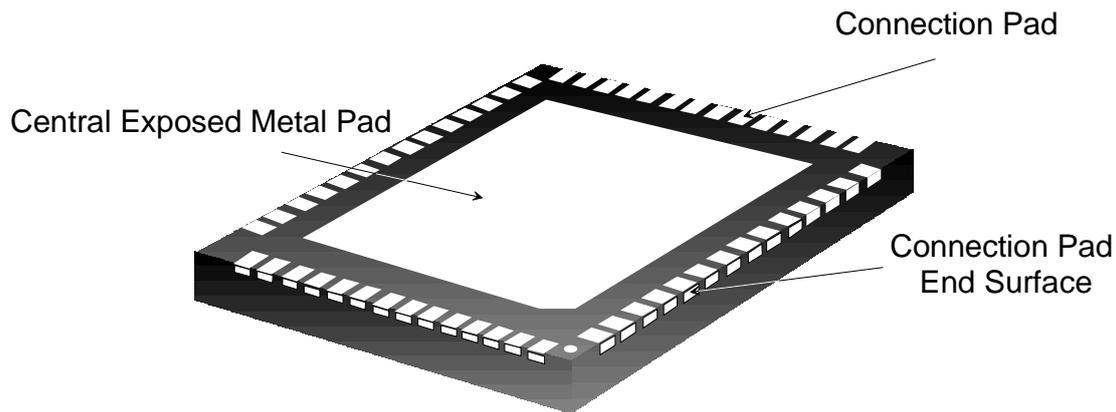


Figure 2

Electrical contact is via rectangular pads around the perimeter of the underside of the package where there is also a large central exposed metal pad. This may be electrically connected to ground for optimum electrical performance¹ and may form an efficient heat sink for devices requiring heat dissipation. For added strength the central exposed metal pad should ideally be soldered to the PCB in addition to the pins. The dot in the corner of the package and/or the cut off corner of the central exposed metal pad indicates the position of pin one. *Please refer to the package diagram/s on a relevant CML product datasheet or see the 'packages' webpage (Products/Packs/Index.htm) on the CML website.*

The package is fabricated in a matrix form and each is segregated either by stamping or sawing. The lead exposed on the side of the package (connection pad end surface) is thus not plated. Solder wetting and electrical connection to the sides of the QFN are not guaranteed. The solderable electrical connection to the perimeter connection pads is made on the bottom of the package.

¹ Certain CML products *require* an electrical connection to ground. This requirement will be stated in the Data Sheet packaging information.

5. Printed Circuit Board Design Guidelines

1. Solder Pad and Solder Mask - Central Exposed Metal Pad

1. The pad on the PCB should match the size of the central exposed metal pad of the package.
2. The solder mask around the pad may be Solder Mask Defined (SMD)² or Non-Solder Mask Defined (NSMD)³ whichever is considered suitable to prevent solder bridging to the pads.
3. The recommended design gap between the PCB ground pad and land pad is 0.15mm minimum but, where space allows, a gap of 0.25mm or more is preferred.
4. Plated thru via holes in the PCB pad should be 0.33mm diameter and plugged. If via holes cannot be plugged, it is recommended to seal the vias on the backside of the board with solder mask material to prevent solder wicking through the holes

2. Solder Pad and Solder Mask - Connection Pads

1. The PCB land width should be the same, or wider than the package connection pad width. To prevent solder bridging, the PCB land should not extend beyond the package connection pad width by more than 0.05mm in either direction.
2. The PCB land length should be the length of the package connection pad plus 0.2mm – 0.5mm beyond the package edge, plus 0.03mm - 0.05mm towards the central exposed metal pad.
3. A Non Solder Mask Defined (NSMD)³ approach is preferable as this allows the solder to wrap around the sides of the pads on the PCB for a reliable solder joint.

² Solder Mask Defined (SMD): Solder mask openings smaller than metal pads.

³ Non-Solder Mask Defined (NSMD): Solder mask openings larger than metal pads.

3. Solder Screen and Reflow Considerations

1. The solder joint thickness for QFN terminations should be 50µm-75µm.
2. A stainless steel stencil, 0.100–0.150 mm thick, is suggested for solder paste application, but actual thickness will be dependant on other components on the board.
3. For better paste release, the aperture walls should be trapezoidal and have the corners rounded.
4. For the connection pads, the stencil opening should match the PCB pad width, but may need to be reduced in length.
5. For the central exposed metal pad area, it is recommended to screen the solder paste in an array of small openings rather than one large opening. The total (cumulative) area of all of the openings should be approximately equal to 50% of the total central exposed metal pad area. This will ensure good solder coverage with fewer voids and avoid the device “floating” on the central exposed metal pad.
6. The solder reflow profile will be dependent on PCB design; PCB thickness; the type of components on the board; the component density, and the recommended profile of the solder paste being used.
7. The typical reflow profile for QFN can be found in the ‘*Solder Profiles*’ document available from the ‘*Packages*’ webpage (*Products/Packs/Index.htm*) or the *datasheet download page* (*Products/Datasheets/Downloads*) on the CML website.
8. A reflow profile may need to be developed for each PCB type using VQFN packages.

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