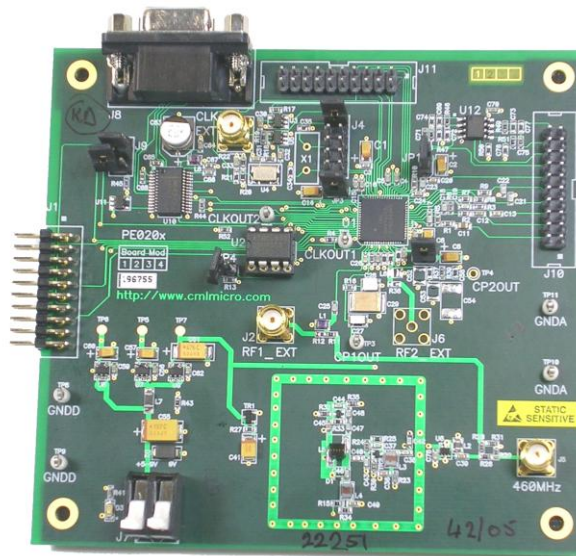


UM0201/8 May 2012

Features

- **CMX703x/CMX713x FirmASIC[®] product range evaluation**
- **Evaluate both RF and baseband capabilities**
- **On-board 460MHz VCO**
- **On-board supply regulators operate from a single 5 volt supply**
- **Command and control by PC via the PE0002 interface card or user's μ C development application or emulator**
- **Serial memory option for Function Image[™] with in-circuit programming**
- **On-board access to all CMX7130 signals, commands and data**



1. Brief Description

The PE0201 Platform Evaluation Kit is designed to assist in the evaluation and application development of the CMX703x/CMX713x FirmASIC[®] products. The kit is in the form of a populated PCB comprising a CMX7130 IC and appropriate supporting components and circuitry, including a 460MHz VCO operating in conjunction with one of the IC's on-chip synthesisers.

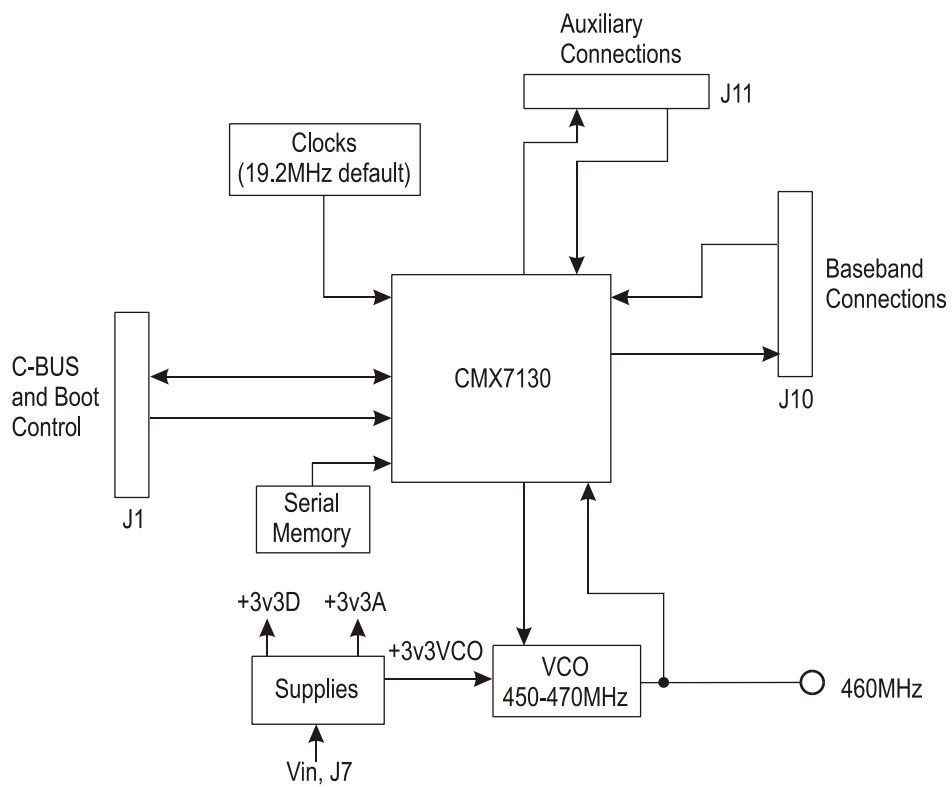
The board also incorporates all the necessary power-supply regulation facilities for operation from a single 5 volt supply, together with a number of board jumpers to enable various circuit arrangements to be effected.

The board is fitted with connectors allowing the PE0201 to be operated with a CML PE0002 Interface Card and associated PC GUI software, or by direct connection between the CMX7130 C-BUS serial port and the user's μ C development application or emulation system.

The 703x or 713x Function Image[™] (FI) can be loaded, on power-up, directly into the on-board target CMX7130 IC using the PE0002 interface or the user's system. Alternatively, it can be pre-loaded, separately, into the on-board serial memory for automatic operation on power-up. Function images can be downloaded from the CML website.

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It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

**Figure 1 Block Diagram**

2. Preliminary Information

The CMX7130 IC fitted to the PE0201 is a special evaluation IC with the architecture of all CMX703x/CMX713x series ICs. The functionality of this evaluation IC is obtained from the relevant Function Image™ (FI); evaluation FIs are downloaded from the CML Technical Portal. Each Function Image™ can represent a different set of features.

2.1 Laboratory Equipment

The following laboratory equipment is needed to use this evaluation kit:

A 5 volt dc regulated power supply.

If being used with the PE0002 Interface Card the following items will also be required.

1. An IBM compatible PC equipped with a USB port and with one of the following Microsoft operating systems installed: 2000sp4 or XPsp2.
2. PE0002 driver and software application ES000221.exe, or later version, installed on the PC. These are available from the CML website as part of the PE0002 support package.
3. USB type A male to mini B male cable.

2.2 Precautions

Like most evaluation kits, this product is designed for use in office and laboratory environments. The following practices will help ensure its proper operation:

2.2.1 Static Protection

This product uses low power CMOS circuits which can be damaged by electrostatic discharge. Partially damaged circuits can function erroneously, leading to misleading results. Observe ESD precautions at all times when handling this product.

2.2.2 Contents - Unpacking

Please ensure that you have received all of the items listed on the separate information sheet (EK0201) and notify CML within 7 working days if the delivery is incomplete.

2.3 Approvals

This product is not approved to any EMC or other regulatory standard. Users are advised to observe local statutory requirements, which may apply to this product and the radio frequency signals that may emanate from it.

3. Quick Start

This section is divided into two sub-sections. The first is for those users who are using the PE0201 with a PE0002 interface card and its Windows PC application. The second is for users who are using the PE0201 by itself, without the PE0002.

3.1 With PE0002

Note that the C-BUS connector J1, a right angle header, of the PE0201 is designed to plug directly into socket J1 of the PE0002.

3.1.1 Setting-Up

The PE0002 driver and software must be installed following the instructions given in the PE0002 user manual.

On the PE0201:

- Ensure that all pins of header, J9, are open circuit.
- Connect the C-BUS header J1 into the mating connector J5 (C-BUS1) on the PE0002.
- Connect 5 volts power to both boards and switch on.
- Run the application ES0002xx.exe
- Press the reset switch (SW1) on the PE0002 board if requested.

The basic arrangement, when used with the PE0002 is shown below.

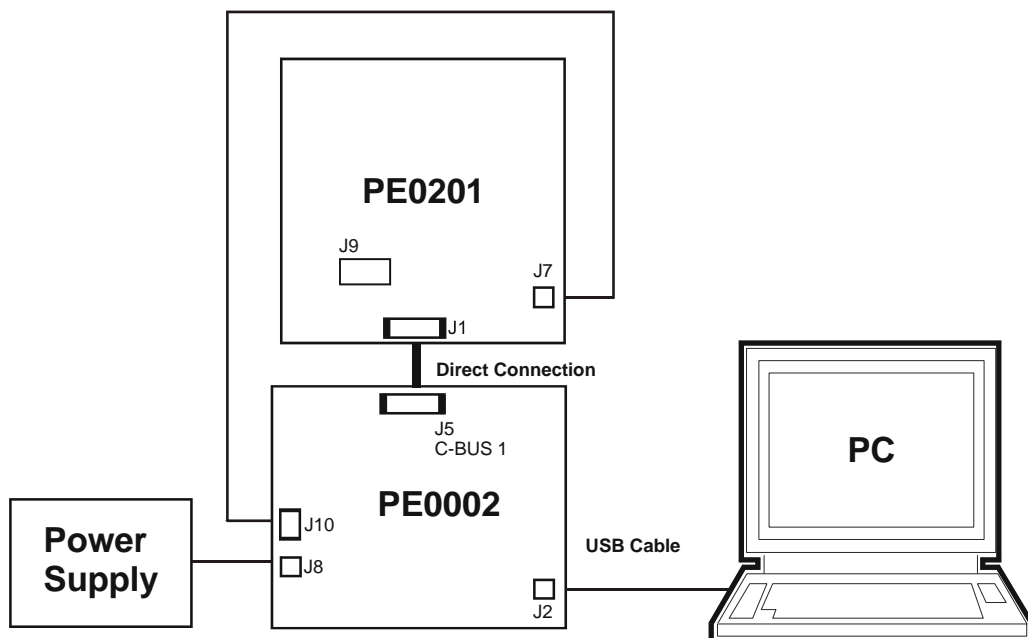


Figure 2 PE0201 used with PE0002

3.1.2 Operation

The Function Image™ (FI) must now be downloaded to the CMX7130 device. Use the 'Function Image Download' tab of the PE0002 windows application. Two methods are available for downloading the FI:

- Directly from a file on the PE0002 host PC to the CMX7130.
- From the PE0201 serial memory. To use this method the serial memory must first be programmed using the 'Program Serial Memory' tab of the PE0002 GUI.

Function Images are available as a 'C' type header file and must be obtained from the CML website.

The PE0201 should now be ready for evaluation of the CMX7130 with the chosen FI.

3.2 Without PE0002

As an alternative to using the PE0002 controller kit, users may control the CMX7130 target device with a user-supplied host interface card. C-BUS serial interface connections are made via connector J1.

The power-up, or boot state of the CMX7130 may be set using BOOTEN1 and BOOTEN2 signals at connector J1 pins 13 and 14 respectively. Alternatively patch cables (not supplied) could be connected at header J9, pins 4 and 6 respectively. Note, the use of jumpers on header J9 pins 3 to 4 and pins 5 to 6 will be in-effective.

A FI for the CMX7130 device must be either included in the customers host system and downloaded to the CMX7130 device on power-up or programmed into the on-board serial memory following the guidelines in the application note: 'Writing a Function Image™ to Serial Memory'.

4. Signal Lists

CONNECTOR PINOUT					
Connector Ref.	Connector Pin No.	Signal Name	Signal Type	Description	
J1	1	N/C	-		
	2	CSN	I/P	Chip select. Connects to host μ C.	
	3	N/C	-		
	4	CDATA	I/P	Serial Data input. Connects to host μ C.	
	5	N/C	-		
	6	SCLK	I/P	Serial clock input. Connects to host μ C.	
	7	N/C	-		
	8	RDATA	O/P	Serial data output. Connects to host μ C.	
	9	N/C	-		
	10	IRQN	O/P	Interrupt request. Connects to host μ C.	
	11, 12	GNDD	PWR	Digital supply ground.	
	13	BOOTEN1	O/P	CMX7130 Hardware Boot Control.	
	14	BOOTEN2	O/P	CMX7130 Hardware Boot Control.	
	15	RS232/CBUSN	O/P	CMX7130 Hardware Boot Control.	
	16	N/C	-	Do not connect to this pin.	
	17	SSOUT/FSO	BI	SSP Frame sync.	
	18	N/C	-	Do not connect to this pin.	
	19, 20	+3V3D	PWR	3.3V dc digital supply rail.	
	J2		RF1_EXT	I/P	External input option to RF synthesiser 1.
	J3		CLK EXT	I/P	External input option for CMX7130 clock.
J5		460MHz	O/P	Output from 460MHz VCO.	
J6		RF2_EXT	I/P	External input to RF synthesiser 2 (not fitted).	
J7		+V	PWR	External supply voltage.	
		GNDD	PWR	External supply ground.	

CONNECTOR PINOUT				
Connector Ref.	Connector Pin No.	Signal Name	Signal Type	Description
J8	1	N/C	-	Do not connect to this pin.
	2	TXD	O/P	9-pin D Type connector – PC TXD.
	3	RXD	I/P	9-pin D Type connector – PC RXD.
	4	N/C	-	Do not connect to this pin.
	5	GNDD	Power	9-pin D Type connector – PC GND.
	6	N/C	-	Do not connect to this pin.
	7	RTS	I/P	9-pin D Type connector – PC RTS.
	8	CTS	O/P	9-pin D Type connector - PC CTS.
	9	N/C	-	Do not connect to this pin.
J10	1	IP1	I/P	Channel 1 inverting input.
	3	IP2	I/P	Channel 2 inverting input.
	5	IP3	I/P	Channel 3 inverting input.
	7	MOD1	O/P	Channel 1 output.
	9	MOD2	O/P	Channel 2 output.
	11	AUDIO	O/P	Channel 3 output.
	13	BUF1IN	I/P	High impedance buffered input.
	15	BUF1OUT	O/P	Buffered output.
	17	BUF2IN	I/P	High impedance buffered input.
	19	BUF2OUT	O/P	Buffered output.
	2, 4, 6, 8, 10, 12, 14, 16, 18, 20	GNDA	PWR	Analogue supply ground.
J11	1	AUXADC4	I/P	Auxiliary ADC input.
	2	AUXDAC1	O/P	Auxiliary DAC output.
	3	AUXADC3	I/P	Auxiliary ADC input.
	4	AUXDAC2	O/P	Auxiliary DAC output.
	5	AUXADC2	I/P	Auxiliary ADC input.
	6	AUXDAC3	O/P	Auxiliary DAC output.
	7	AUXADC1	I/P	Auxiliary ADC input.
	8	AUXDAC4	O/P	Auxiliary DAC output.
	9, 10	GNDA	PWR	Analogue supply ground.

CONNECTOR PINOUT				
Connector Ref.	Connector Pin No.	Signal Name	Signal Type	Description
	11, 12	N/C		Do not connect to these pins.
	13, 14	GNDD	PWR	Digital supply ground.
	15, 16	N/C	-	Do not connect to these pins.
	17	SSOUT/FSO	BI	SSP Frame sync.
	18	N/C	-	Do not connect to this pin.
	19	GPIO2	BI	General purpose I/O pin.
	20	GPIO1	BI	General purpose I/O pin.

TEST POINTS		
Test Point Ref.	Default Measurement	Description
TP1	-	CMX7130 system clock 1 output.
TP2	-	CMX7130 system clock 2 output.
TP3	-	CP1OUT, charge pump output for RF synthesiser 1.
TP4	-	CP2OUT, charge pump output for RF synthesiser 2 (TP4 not fitted).
TP5	3.3V	Output from on-board regulator. DC supply voltage for analogue rail.
TP6	3.3V	Output from on-board regulator. DC supply voltage for digital rail.
TP7	3.3V	Output from on-board regulator. DC supply voltage for RF Charge Pump and 460MHz VCO.
TP8	0V	GNDD, digital ground.
TP9	0V	GNDD, digital ground.
TP10	0V	GNDA, analogue ground.
TP11	0V	GNDA, analogue ground.

JUMPERS/LINKS			
Link Ref.	Positions	Default Position	Description
JP1	1-2	short	Isolates analogue supply rail from CMX7130.
JP2	1-2	short	Isolates charge pump supply rail from CMX7130.
JP3	1-2	short	Isolates digital supply rail from CMX7130.
J4	1-2	short	19.2MHz TXCO clock source.
	3-4	open	External clock source.
	5-6	open	Crystal clock source – if components fitted by customer.
	7-8	short	Ground external clock input.
	9-10	open	Crystal clock source – if components fitted by customer.
J9	1-2	open	Manual C-BUS (open) or RS232 selection (short).
	3-4	open	Do not use.
	5-6	open	Do not use.
J10	13-14	short	Ground input to uncommitted buffer1.
	17-18	short	Ground input to uncommitted buffer2.

LEDs	
LED Ref.	Description
D16	Indicates that digital supply voltage is present.

Notes: I/P = Input
O/P = Output
BI = Bidirectional
N/C = Not connected
PWR = Power supply connection

5. Circuit Schematics and Board Layouts

For clarity, circuit schematics are available as a separate high resolution pdf file. This can be found on the CML website.

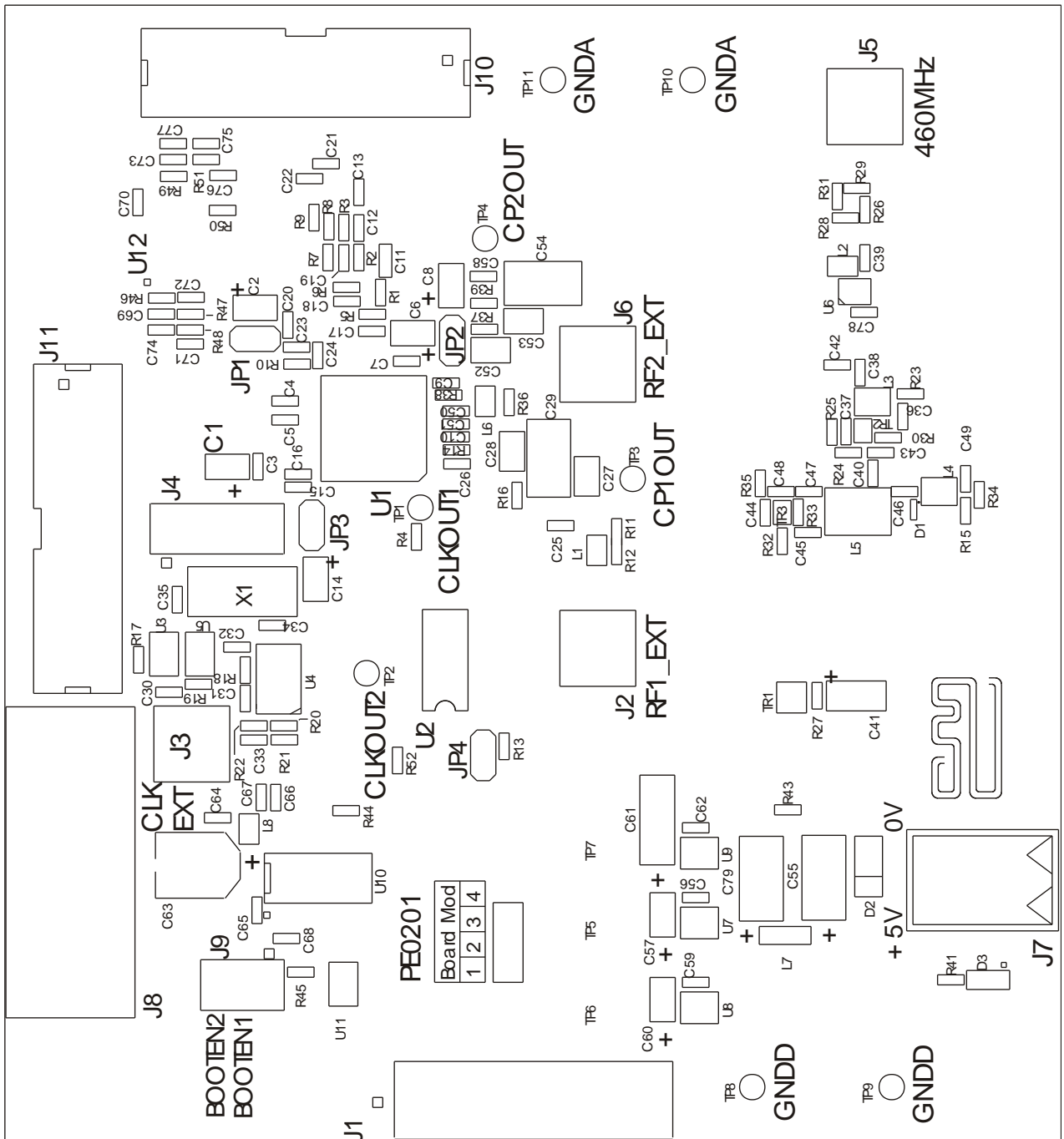


Figure 3 Evaluation Board – Layout

6. Detailed Description

6.1 Hardware Description

The PE0201 as shipped may not have the optimum configuration or component values for all function images. Check the PE0201 schematic against recommendations in the specific CMX703x/CMX713x datasheet.

6.1.1 Power supplies

The board is fitted with three voltage regulators. U7, U8 and U9 provide the analogue, digital and RF Charge Pump supply rails respectively. The input to these three regulators is provided by an external 5V dc regulated power supply, which is connected to the board via connector J7, a snap type connector.

The analogue, digital and RF Charge Pump supply voltage levels can be monitored on test points TP5, TP6 and TP7 respectively.

LED illumination confirms the on-board presence of the +3.3V dc digital voltage supply.

6.1.2 Clock Options

The PCB is designed to provide three CMX7130 device clock options. The board is supplied with a 19.2MHz oscillator module fitted. This option allows convenient RF synthesiser configuration to typical channel spacings. If a FI providing an auxiliary DAC at AuxDAC4 is used, then fine tuning of the output frequency is possible. A 3.9k Ω resistor should be fitted in position R21 for this purpose.

Other options are an external clock source at J3 and PCB footprints for assembly of a quartz crystal oscillator circuit (C34, C35 and X1).

Header J4 is used with jumper sockets to select the required option as shown in the table below. Shaded cells illustrate locations where a jumper socket should be fitted.

J4 Jumper position	Clock option		
	19.2MHz TCXO (default)	External	Quartz crystal
1->2			
3->4			
5->6			
7->8			
9->10			

Table 1 Clock Select Jumper Positions

6.1.3 Control Interface

The C-BUS and CMX7130 boot control signals are brought out on connector J1. This is a right-angle male header designed to plug directly into the PE0002 interface card which has a matching female header

Alternatively, if not using the PE0002 the boot state of the CMX7130 can be set using patch cables (not supplied) connected at header J9, pins 4 and 6.

Some CMX703x/CMX713x Function Images will have an RS232 interface instead of a C-BUS interface. In such cases, the PE0201 will not operate with the PE0002 interface card; the RS232 interface provided on the PE0201 PCB should be used instead. RS232 mode for the CMX7130 can be selected by shorting pins 1 and 2 of header J9 with a jumper.

6.1.4 Serial Memory

The serial memory, U2, can be used for non-volatile storage of a Function Image™. The PE0201 is shipped with a blank serial memory.

6.1.5 Baseband Interfacing

Connector J11 provides access to Auxiliary ADCs 1 to 4, Auxiliary DACs 1 to 4, and the general purpose I/O lines of the CMX7130 device.

The CMX7130 device baseband input amplifiers for IP1, IP2 and IP3 are configured as ac coupled, unity gain, inverting amplifiers. The inputs to these circuits are fed from connector J10. For some function images, it is desirable to dc couple the inputs IP1, IP2 and IP3 by replacing capacitors C11, C12 and C13 with zero ohm links.

The CMX7130 device baseband outputs, MOD1, MOD2 and AUDIO, are fed through an RC network to connector J10.

A dual op amp IC is fitted to the board, with both amplifiers configured as unity-gain buffers. It is possible to set up other op amp based configurations with the addition of passive components to the PCB footprints provided. It is recommended that 0603 sized surface mount components are used. Access to the input and output of each of these uncommitted amplifiers is also from connector J10.

6.1.6 Digital Interfacing

Connector J11 provides access to two general purpose I/O lines.

Some CMX713x Function Images have operational modes which use the synchronous serial port of the CMX7130 device. The relevant signals can be found on the PE0201 according to the following table:

SSP Signal	PE0201 Signal Name	PE0201 Location
FSO/SSOUT	FSO	J11 pin 17
SDI (MISO)	EPSO	U2 pin 2
SDO (MOSI)	EPSI	U2 pin 5
EPSCCLK	EPSCCLK	U2 pin 6

Table 2 SSP Signal Mapping

Use of these signals is Function Image™ dependant. In some cases they will have no function. See relevant CMX703x/CMX713x documentation.

6.1.7 RF Circuits

The board is fitted with a Voltage Controlled Oscillator (VCO). Using RF synthesiser 1 of the CMX7130 device, the VCO is tuneable across a range of 455 to 465 MHz, with a nominal frequency of 460MHz. The output of the VCO is fed to connector J5, which is a straight SMA type. The charge pump settings for CMX703x (RF channel control register, \$B3), when using this VCO should be:

Positive slope - \$B3;b4=0.

High gain - \$B3;b3=1;

For further information, refer to relevant CMX703x/CMX713x data sheet.

Alternatively, RF synthesiser 1 can be used with an external VCO, with the following circuit changes:

- Remove R11 and R28 - Disconnect VCO output from CMX703x
- Remove R32 – Stops the on-board VCO oscillating
- Remove R15 – Disconnect CMX7130 charge pump output from on-board VCO

The charge pump output of RF synthesiser 1 can now be picked up from TP3, labelled CP1OUT, and the users VCO output connected to the SMA connector J2, labelled RF1_EXT. Note that the loop filter for RF synthesiser 1 is still in circuit.

RF synthesiser 2 can also be used with a user-supplied external VCO. A loop filter can be constructed using the PCB footprints provided. Also, the ISET resistor, R38, must be fitted. The user-supplied VCO can be fitted across the following connectors that are not fitted:

- J6, SMA socket, labelled RF2_EXT – RF input to RF synthesiser 2
- TP4, test loop, labelled CP2OUT – Charge pump output

6.2 Function Image™

There are two methods by which a FI may be loaded into the CMX7130 device.

Whenever power is removed from the PE0201 the FI data will be erased from the CMX7130 device. Therefore, whenever power is applied a FI must be loaded, either from the serial memory or via the C-BUS interface.

If the PE0201 is used with the PE0002 PC interface, function images can be loaded as follows:

6.2.1 Load Function Image™ via C-BUS

Use the Function Image Load tab. Select Function Image Source: "C-BUS".

- Enter the name of the file containing the Function Image™, or navigate to the required file name using the 'Browse' button
- Enter the activation code in the lower edit box. Alternatively select one of two previously used codes in the drop down list
- Select Target Board
- Click the "Load" button. The progress of the download is shown visually on the progress bar and when the download has completed a message box will be displayed indicating if the result of the download operation was successful or not.

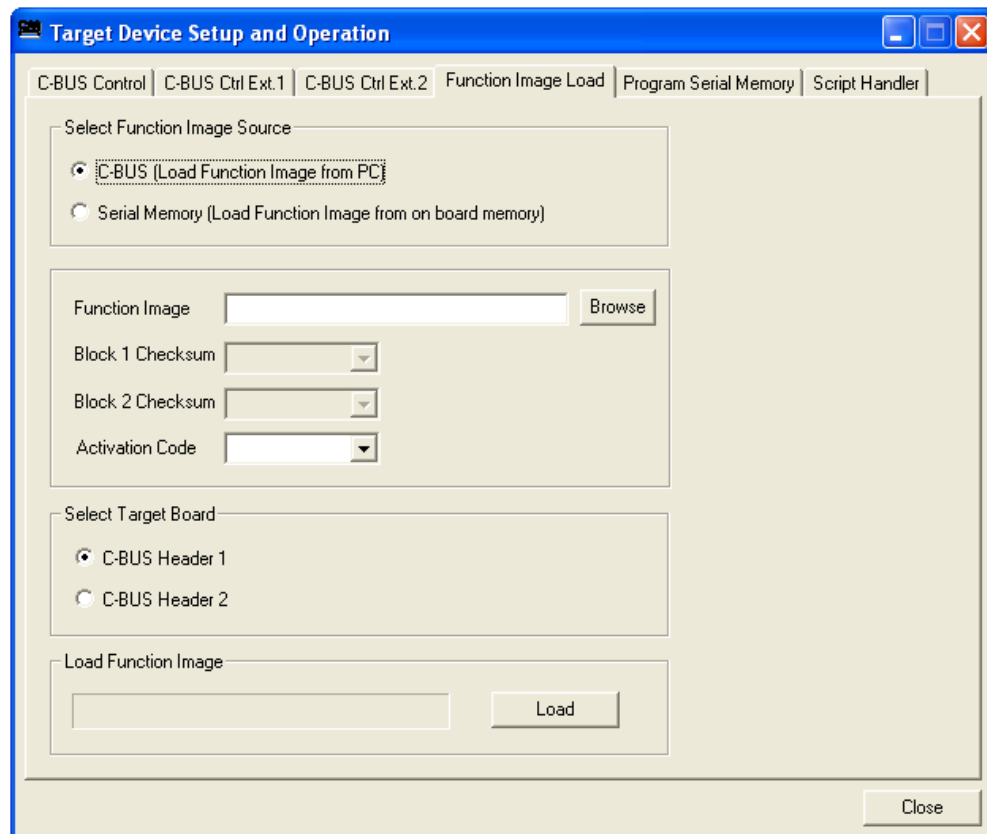


Figure 4 Function Image Load Tab – via C-BUS

6.2.2 Load Function Image™ from Serial Memory Device

It is assumed that the serial memory has been programmed with the Function Image™ prior to using this load method. This can be carried out with the serial memory in circuit using the ES0002xx 'Program Serial Memory' tab.

Use the Function Image Load tab. Select Function Image Source: "Serial Memory".

- Enter the block 1 and block 2 checksum values in the edit boxes. Alternatively select one of two previously used values in the drop down list for each block
- Enter the activation code in the lower edit box. Alternatively select one of two previously used codes in the drop down list
- Select Target Board
- Click the "Load" button. The progress of the download is shown visually on the progress bar and when the download has completed a message box will be displayed indicating if the result of the download operation was successful or not

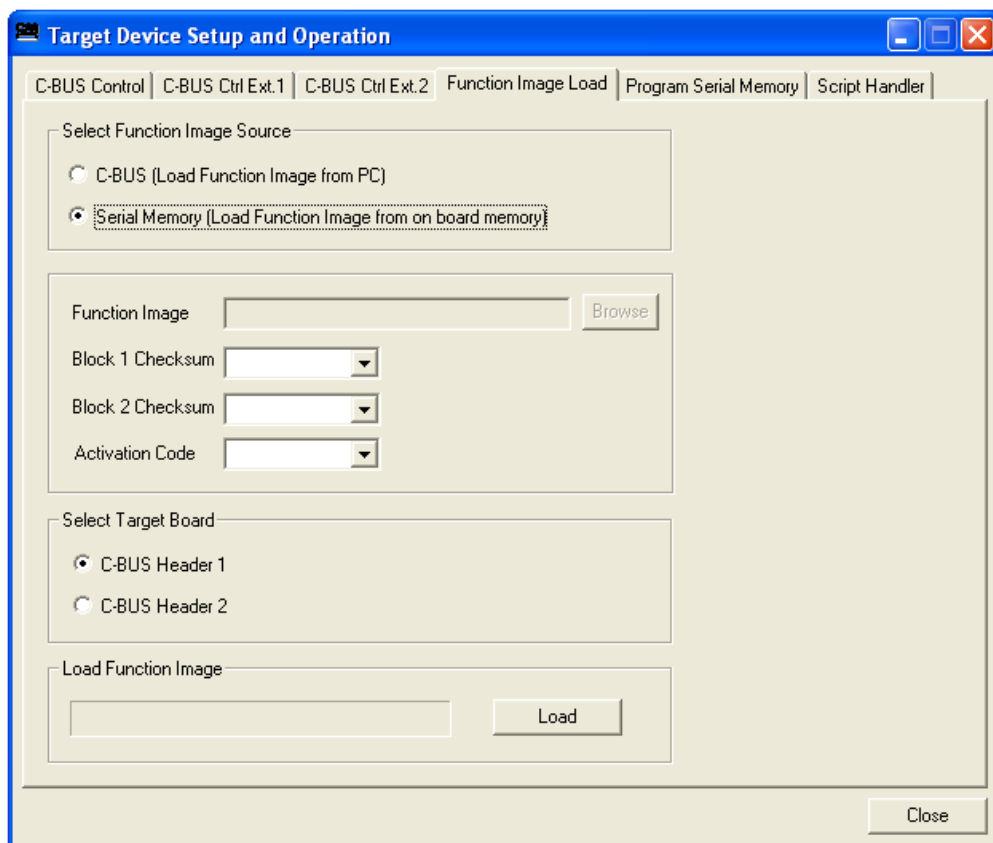


Figure 5 Function Image Load Tab – From Serial Memory

6.2.3 Program Serial Memory

The specific serial memory device fitted to the PE0201 and the appropriate "thick stub" application software are shown below. The "thick stub" application software is available from the CML Technical Portal.

Revision	Serial numbers	Memory type	Thick Stub
Up to Rev F Mod 3*	Up to 198014	Atmel AT25HP512	FI_FLASH_XX.h
From Rev F Mod 4*		ST M25P10A or equivalent.	EF0201_M25P10A_XX.h

Table 3 Serial Memory Types

* For correct identification of mod state (modification state) see section 6.5.1

Use the 'Program Serial Memory' tab:

- Enter the name of the file containing the thick stub, or navigate to the required file name using the 'Browse' button. This file is in the same 'C' language header format as the Function Image™
- Enter the name of the file containing the Function Image™, or navigate to the required file name using the 'Browse' button
- Enter, in units of MHz, the crystal/clock input frequency of the CMX7130 device. The default is 19.2MHz. The Clk. Divide Setting is dependent on the entered frequency value and is calculated by the software, requiring no intervention from the user
- Select Target Board
- Click the "Load" button

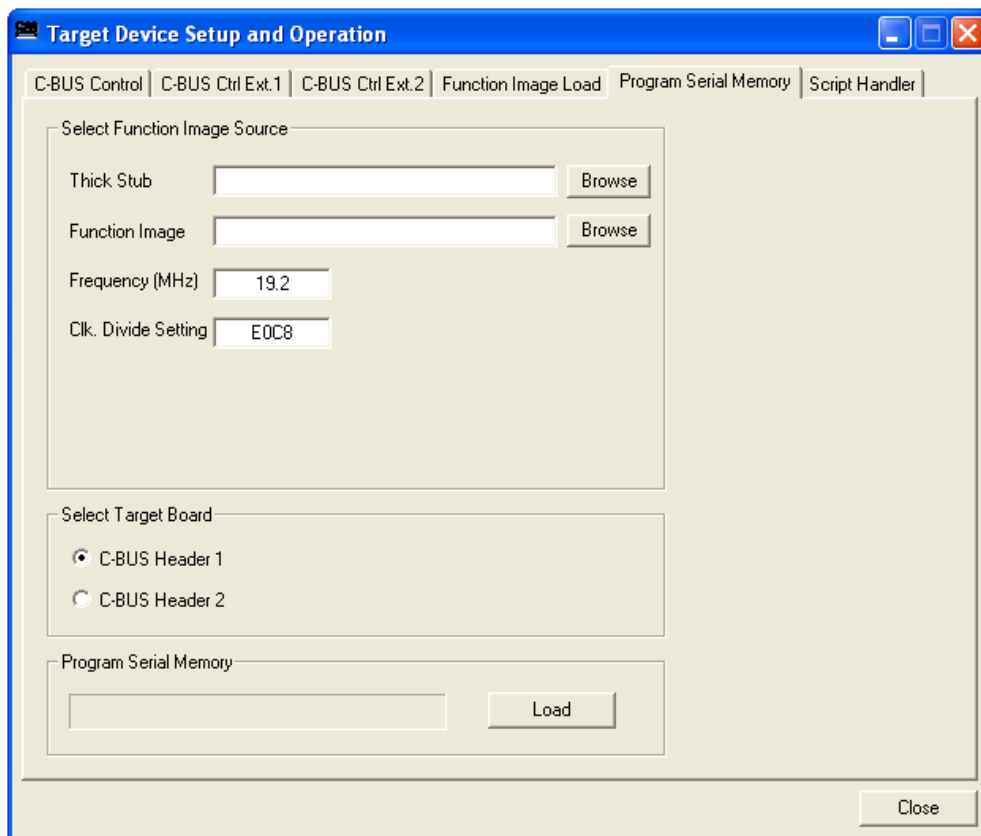


Figure 6 Program Serial Memory Tab

Shortly after pressing the Load button, a message box will confirm that the application has loaded the Thick Stub.



Figure 7 Thick Stub loaded Message Box

Click on the message box OK button and the application will proceed to program the Function Image™ into the serial memory on the PE0201 card. Progress is shown visually on the progress bar. When programming is complete a message box will be displayed indicating if the operation was successful or not.



Figure 8 Program Serial Memory Complete Message Box

6.3 Evaluation Tests

Before a FI is loaded into the CMX7130 device, there is a limited functionality which can be demonstrated directly by programming the C-BUS. The first group of examples can be used to verify control of the CMX7130 via the C-BUS serial interface.

6.3.1 Write to and Read from a Register

- Write any 16-bit number to register \$C0.
The data transferred to the device on the Command Data pin looks like this:

{ C0 }	{ <ms byte> }	{ <ls byte> } Command Data
--------	---------------	---------------	--------------------
- The value written to this register (the Powerdown Control register) can be read back from register \$C4 by issuing a single command byte, then reading two data bytes from the Reply Data pin, as follows:

{ C4 } Command Data
{ <ms byte> }	{ <ls byte> }
 Reply Data

Note that the power consumption of the device will increase once this register has been written to, since some parts of the device will no longer be powersaved.

6.3.2 Check Analogue Path and Set Input Gain

Write 0x4061 to \$C0 (Powerdown Control)
 Write 0x770F to \$B0 (Analogue Gain)
 Write 0x0C30 to \$B1 (Input Gain and Signal Routing)
 Write 0x0008 to \$CF (Test Mode)

Apply a 1kHz, audio signal to the input, IP3 (J10 pin 5), at a level of -10dBm (the maximum signal level before distortion is about +1dBm).

Check the audio signal coming out of the AUDIO OUT pin (J10, pin 11). The level should be 5.5dB below the level of the input signal.

The MOD1 and MOD2 outputs should have no signal on them. All three outputs should have a dc bias level of approximately 1.65 volts.

6.3.3 Check Analogue Path and Set Output Gain

Write 0x03E1 to \$C0 (Powerdown Control)
 Write 0x410C to \$B0 (Analogue Gain)
 Write 0x0001 to \$CF (Test Mode)

Apply a differential 1kHz, audio signal across the inputs, IP1 (J10, pin 1) and IP2 (J10, pin 2), at a level of 0dBm between them. Measure the differential level between IP1FB and IP2FB pins and use this value as a reference to further measurements.

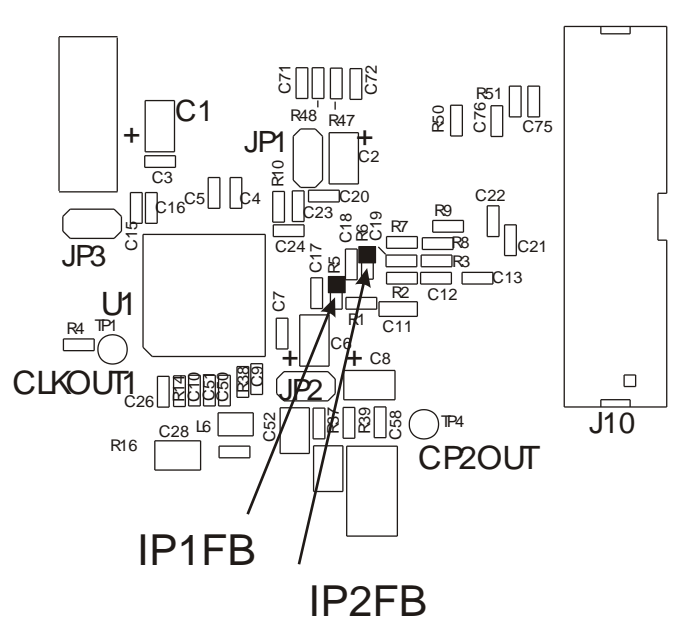


Figure 9 Analogue Path Test – Input Measurement Points

Check the audio signal coming out of the AUDIO OUT pin (J10, pin 11). The level should be -9.6dBm.

Check the audio signal coming out of the MOD1 pin (J10, pin 7). The level should be -6.0dBm.

Check the audio signal coming out of the MOD2 pin (J10, pin 9). The level should be -12.0dBm.

The MOD1 and MOD2 outputs should have a DC bias level of approximately 1.65 volts.

6.3.4 Generate Two External Digital Clocks

Write 0x0021 to \$C0 (Powerdown Control)

Write 0x2577 to \$AB (System Clock 1 PLL Configuration)

Write 0xE0C8 to \$AC (System Clock 1 Reference and Source Configuration)

Write 0x09A0 to \$AD (System Clock 2 PLL Configuration)

Write 0xE0C8 to \$AE (System Clock 2 Reference and Source Configuration)

With the default 19.2MHz clock input, a digital clock frequency of 4.0MHz should be observed at the AUX/SYS CLOCK 1 output, labelled CLKOUT1 (TP1), and a frequency of 19.968MHz should be observed at the AUX/SYS CLOCK 2 output, labelled CLKOUT2 (TP2).

Now write 0xA0C8 to either \$AC or \$AE registers, to turn off the CLKOUT1 or CLKOUT2 outputs, respectively.

6.3.5 Set RF Synthesiser 1

These settings will enable the on-board VCO to switch between two frequencies of 455MHz and 465MHz. The VCO output is monitored at SMA socket, J5, labelled 460MHz.

Each synthesiser has an N and an R value for the Rx frequency and an N and an R value for the Tx frequency. Once programmed, the synthesiser can easily be switched between Rx and Tx. An Application Note is available from the CML website, to help calculate the N and R values.

The RF Channel Data register (\$B2) is used to program both RF synthesisers and this is done by 16 contiguous writes to this register. This can be reduced to 8 contiguous writes if only one of the synthesisers is to be programmed. There is no indication of the completion of these writes, except that the synthesiser which has been written to will indicate lock in the RF Channel Status register (\$B4), once it has been enabled, and providing that the correct external components have been used for the programmed frequency. For this example, it is assumed that the RF frequency is derived from the default clock frequency of 19.2MHz.

To select an Rx frequency of 465MHz and a Tx frequency of 455MHz on Channel 1 Synthesiser, with a loop comparison frequency of 25kHz, the following values of N and R are required:

For 455MHz, using the Tx divider registers:

Tx N = 18,200 = 0x4718

Tx R = 768 = 0x0300

For 465MHz, using the Rx divider registers:

Rx N = 18,600 = 0x48A8

Rx R = 768 = 0x0300

Write 0x8000 to \$B3 (RF Channel Control) to select XTAL clock input as reference.

Write 0x0021 to \$C0 (Powerdown Control)

Write 0x4318 to \$B2 (RF Channel Data, Tx N b9:0)

Write 0x4411 to \$B2 (RF Channel Data, Tx N b19:10)

Write 0x4B00 to \$B2 (RF Channel Data, Tx R b9:0)

Write 0x4C00 to \$B2 (RF Channel Data, Tx R b19:10)

Write 0x50A8 to \$B2 (RF Channel Data, Rx N b9:0)

Write 0x5412 to \$B2 (RF Channel Data, Rx N b19:10)

Write 0x5B00 to \$B2 (RF Channel Data, Rx R b9:0)

Write 0x5C00 to \$B2 (RF Channel Data, Rx R b19:10)

Then:

Write 0x802D to \$B3 (RF Channel Control) to select the Rx frequency or ...

Write 0x802B to \$B3 (RF Channel Control) to select the Tx frequency or ...

Write 0x8028 to \$B3 (RF Channel Control) to disable both Rx and Tx frequencies

When RF Synthesiser 1 is in lock, it will return the value 0x01 in the RF Channel Status register (\$B4). When not in lock, this value will be 0x00. Depending on the setting of the IRQ mask in the IRQ Mask register (\$CE), an interrupt will be generated and the interrupt will be reported in the Status 1 register (\$C6) as the value 0x8002.

6.4 Troubleshooting

After loading a Function Image™, the ES0002xx application writes the activation code that has been typed into the Activation Code edit box to the CMX7130 device.

If this code is incorrect for the Function Image™ that has just been loaded the CMX7130 device will lock up and will not respond to further input from the ES0002xx application.

It is recoverable only by closing the ES0002xx application, power cycling the PE0201 and PE0002 cards, and then restarting the application. Keep the power off for at least 10 seconds during this process.

6.4.1 Modification State

The modification state (mod state) of the PE0201 can be determined from the 'Board Mod' box printed on the PCB silkscreen. The highest number in the box that is blacked out gives the mod state. The following examples indicate a mod state of 3.

Board Mod			
●	●	●	4
5	6	7	8

Board Mod			
■	■	■	4
5	6	7	8

Figure 10 Examples of Mod State Identification

7. Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the Evaluation Kit.

	Min.	Max.	Units
Supply ($V_{IN} - V_{SS}$)	-0.3	9.0	V
Voltage on any connector pin to V_{SS}	-0.3	3.6	V
Current into or out of V_{IN} and V_{SS} pins	0	+0.45	A
Current into or out of any other connector pin	-20	+20	mA

7.1.2 Operating Limits

Correct operation of the Evaluation Kit outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (+V - V_{GND})		4.5	5.5	V
External Clock Frequency		4.0	24.576	MHz

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Evaluation Device Clock Frequency = 19.2MHz, $V_{IN} = 5.0V$, $T_{amb} = +25^{\circ}C$.

For CMX703x/CMX713x parameters, see relevant CMX703x/CMX713x datasheet.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD}	1	60	75	100	mA
+3V3A		3.15	3.3	3.45	V
+3V3D		3.15	3.3	3.45	V
+3V3_VCO		3.15	3.3	3.45	V
Baseband Parameters					
Output Impedances					
MOD1, MOD2 and AUDIO	2	-	100	-	k Ω
BUF1OUT and BUF2OUT	4	-	0.1	-	Ω
Input Impedances					
IP1, IP2 and IP3		-	50	-	k Ω
BUF1IN and BUF2IN	4	1	-	-	M Ω
External Clock Input					
'High' pulse width	3	21	-	-	ns
'Low' pulse width	3	21	-	-	ns
Input impedance		10	-	-	M Ω
VCO output					
Frequency range		455	-	465	MHz
Power		-	6.5	-	dBm
Output Impedance		-	50	-	Ω

- Notes:**
1. Not including any current drawn from pins by external circuitry.
 2. Small signal impedance.
 3. Timing for an external input to the CLOCK/XTAL pin.
 4. When configured, as supplied, as unity gain buffers.

7.1.4 Operating Characteristics – Timing Diagrams

See relevant CMX703x/CMX713x product documentation for C-BUS signal timing information.

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