

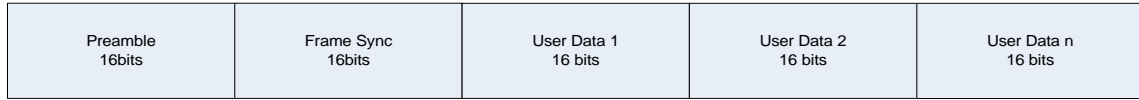
June 2015

The following illustrations and flow-charts demonstrate how the IC transmits and receives FFSK data when using the CMX7031/7041 FI1 Two-Way Radio Processors.

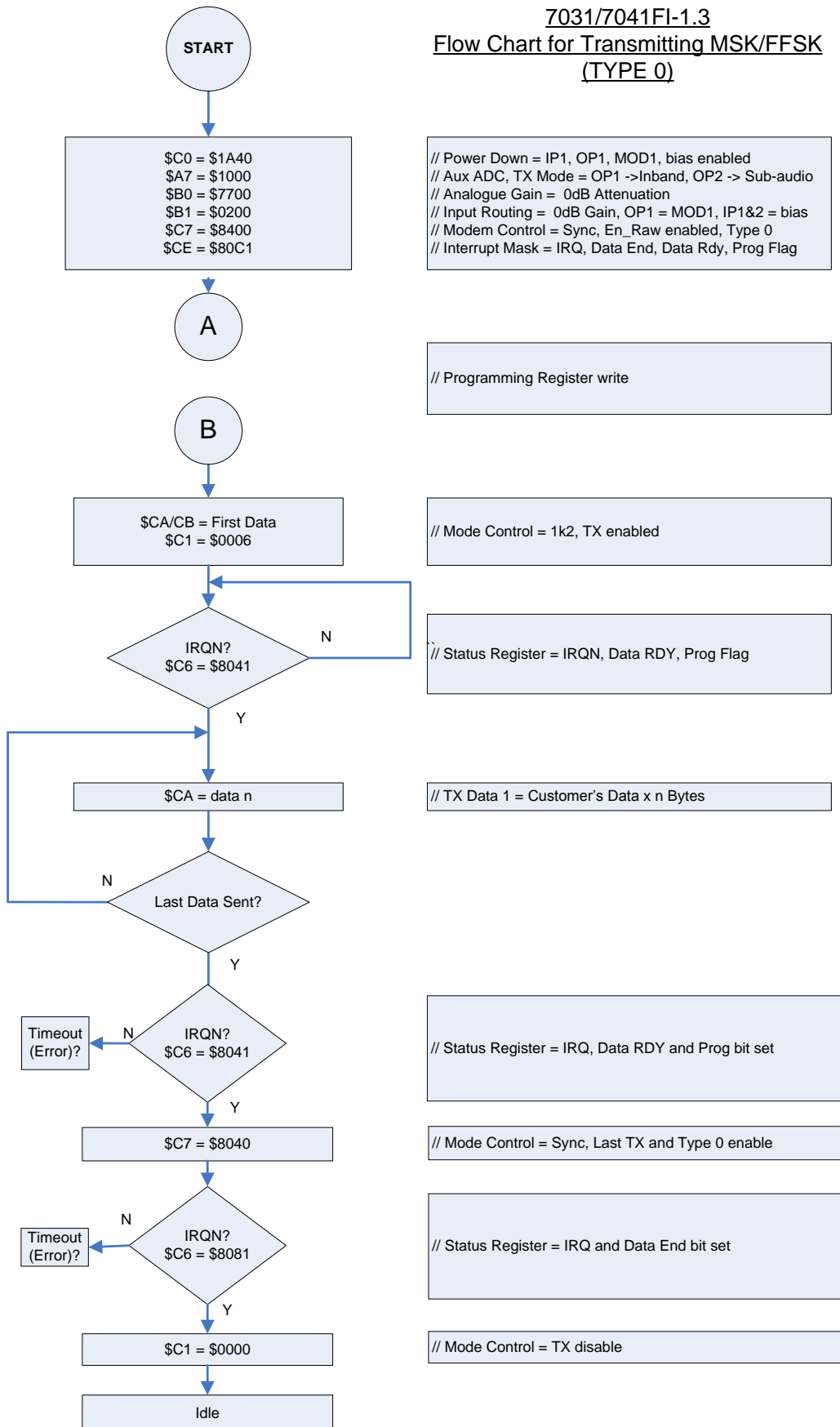
When referring to the following it is assumed that the device will already be powered-up, reset and stable prior to further register set-ups. In addition only those register directly relevant to FFSK data transmission are shown; other CBus settings are not shown (e.g., Synth, SysClock, etc).

Full ISR (Interrupt Service Routine) methods of IRQ handling are recommended during data transfers.

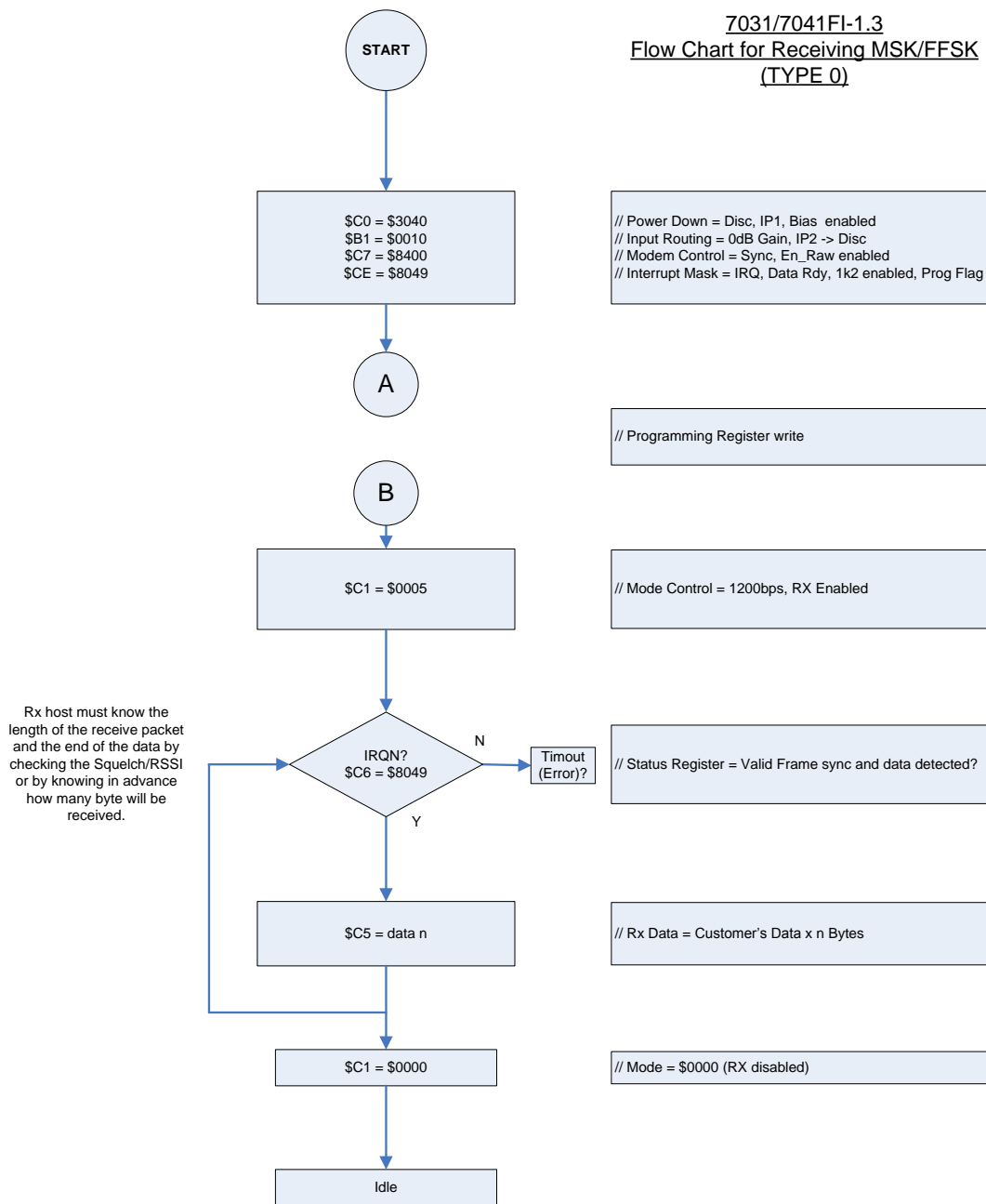
Type 0 data format



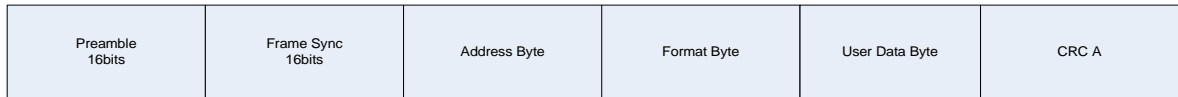
7031/7041FI-1.3 Flow Chart for Transmitting MSK/FFSK (TYPE 0)



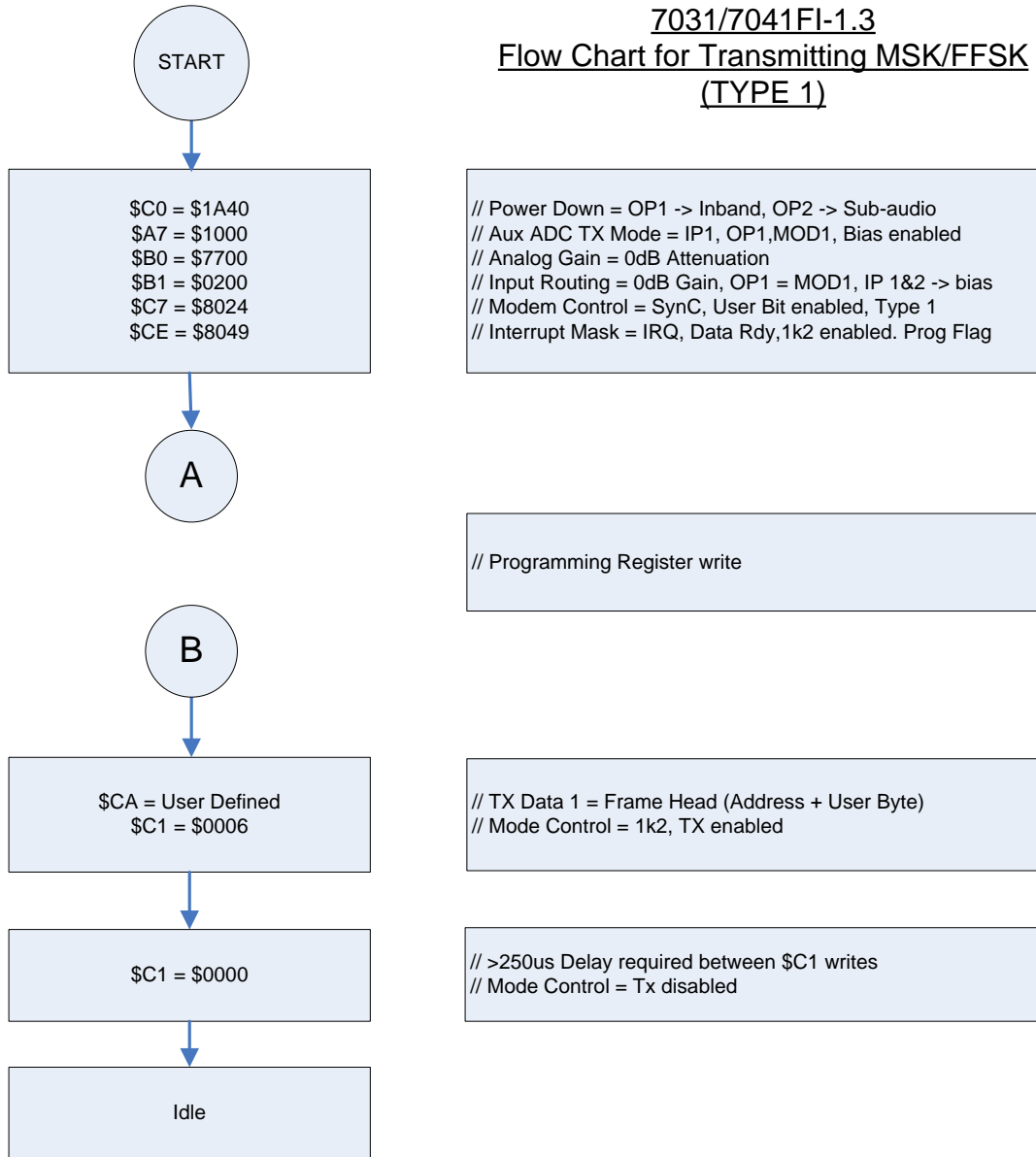
7031/7041FI-1.3
 Flow Chart for Receiving MSK/FFSK
 (TYPE 0)



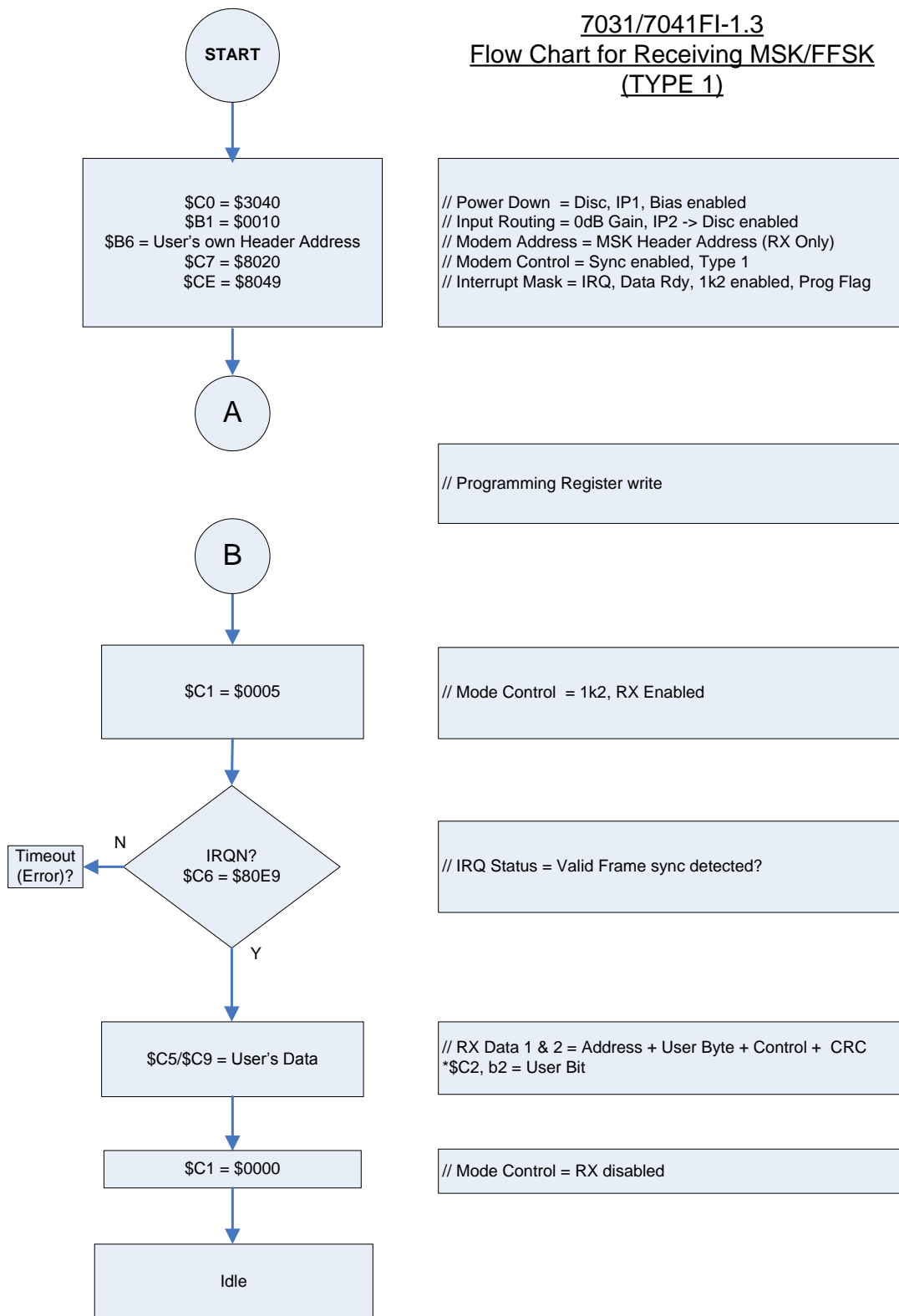
Type 1 data format



7031/7041FI-1.3 Flow Chart for Transmitting MSK/FFSK (TYPE 1)



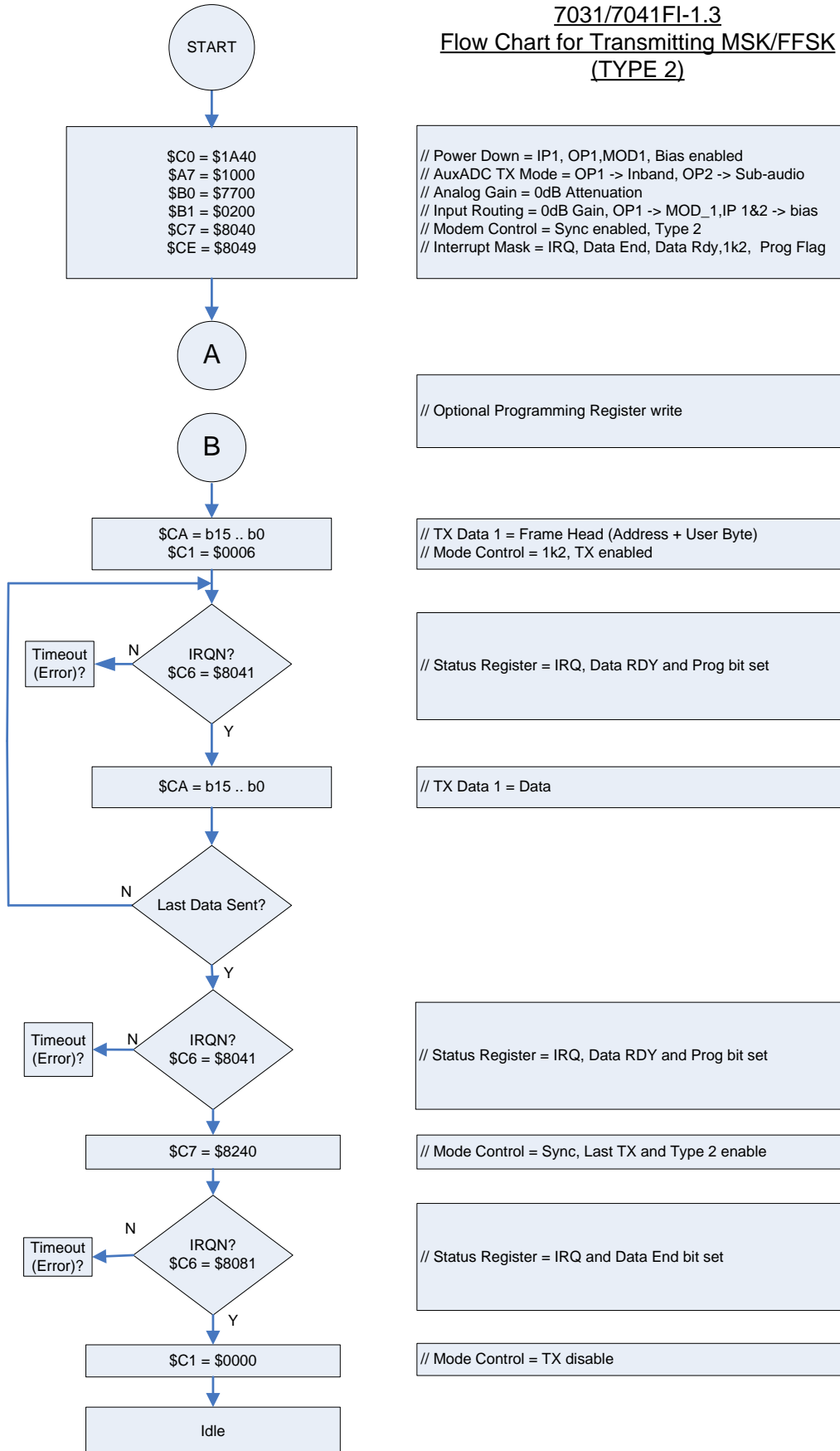
7031/7041FI-1.3
Flow Chart for Receiving MSK/FSK
(TYPE 1)



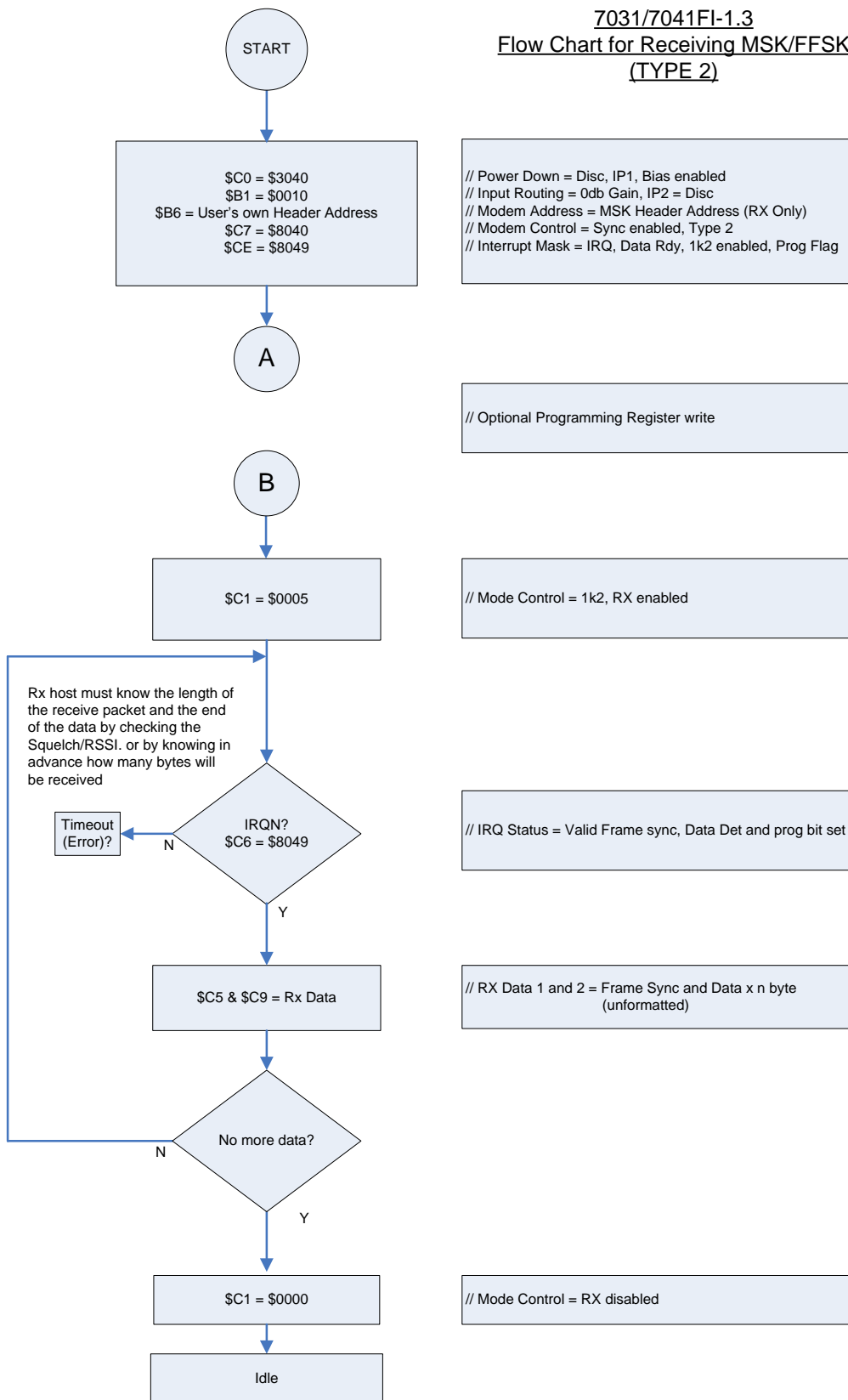
Type 2 data format

Preamble 16bits	Frame Sync 16bits	Address Byte	Format Byte	User Data Byte	CRC A	Data 1 16bits	Data n 16bits
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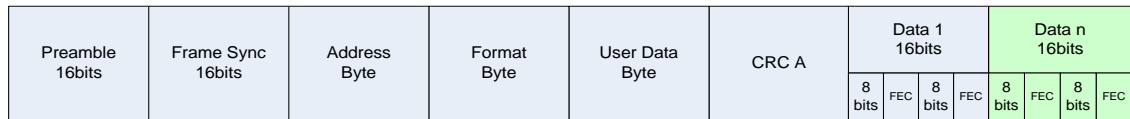
7031/7041FI-1.3 Flow Chart for Transmitting MSK/FFSK (TYPE 2)



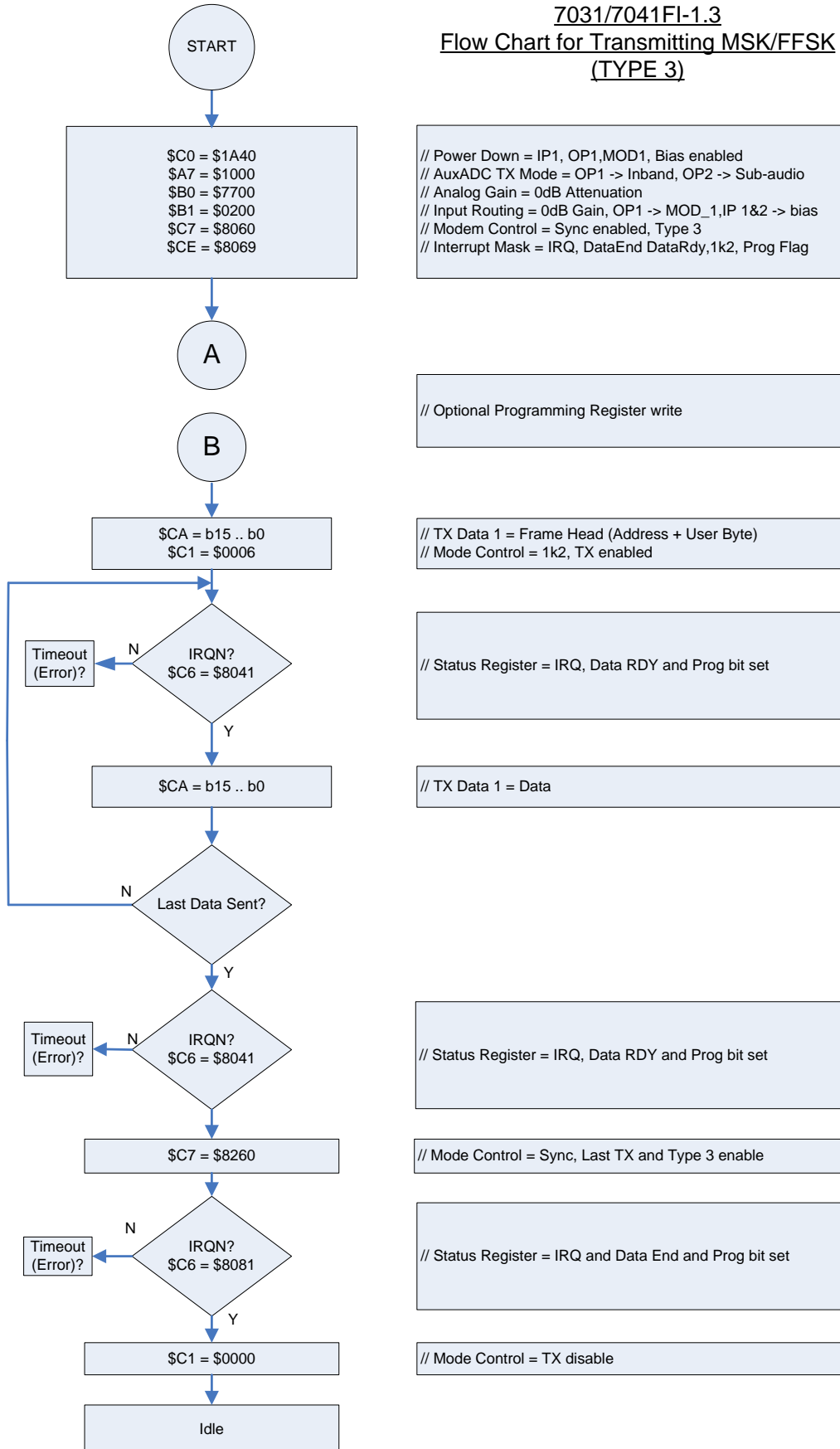
7031/7041FI-1.3
Flow Chart for Receiving MSK/FFSK
(TYPE 2)



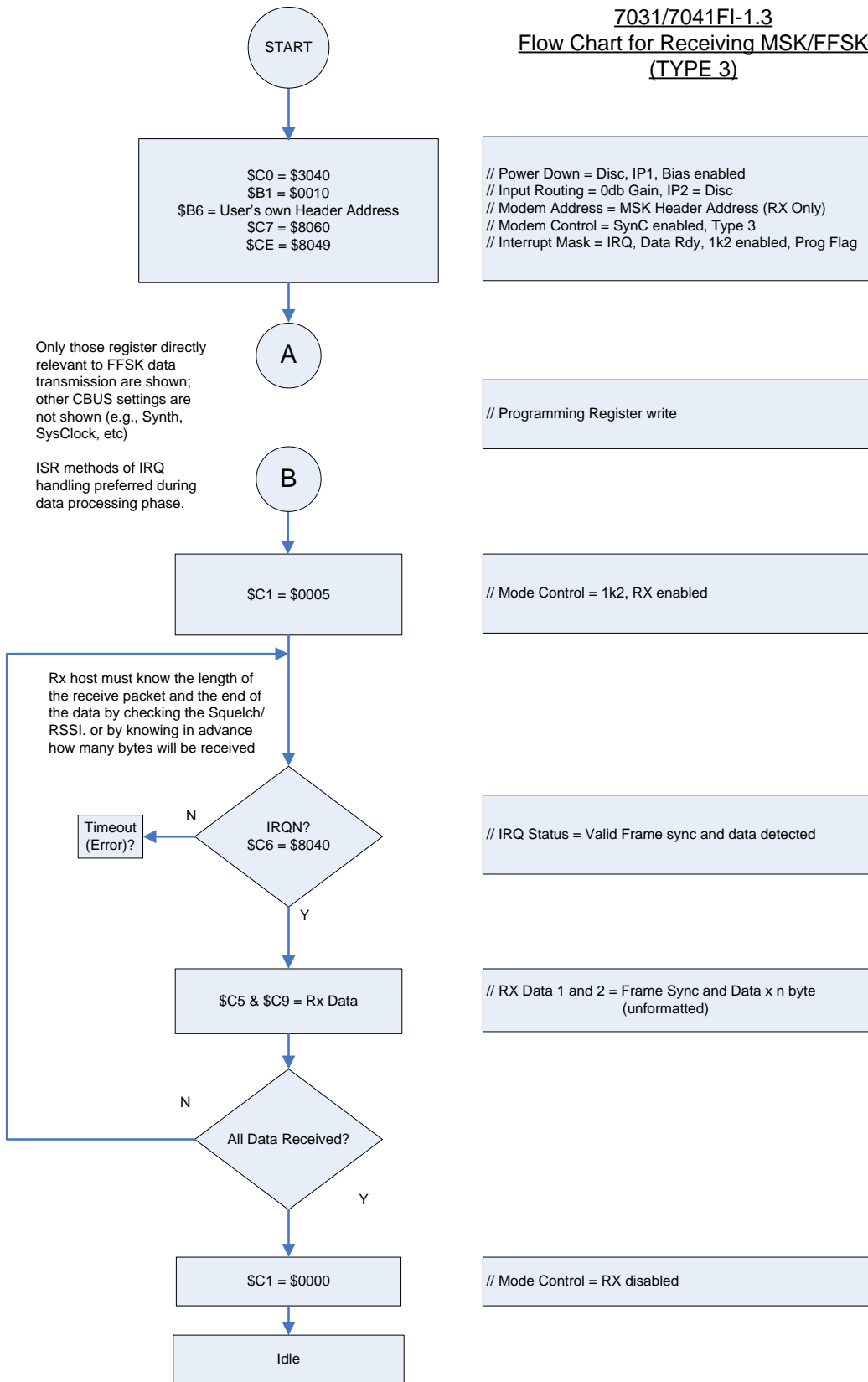
Type 3 data format



7031/7041FI-1.3 Flow Chart for Transmitting MSK/FFSK (TYPE 3)



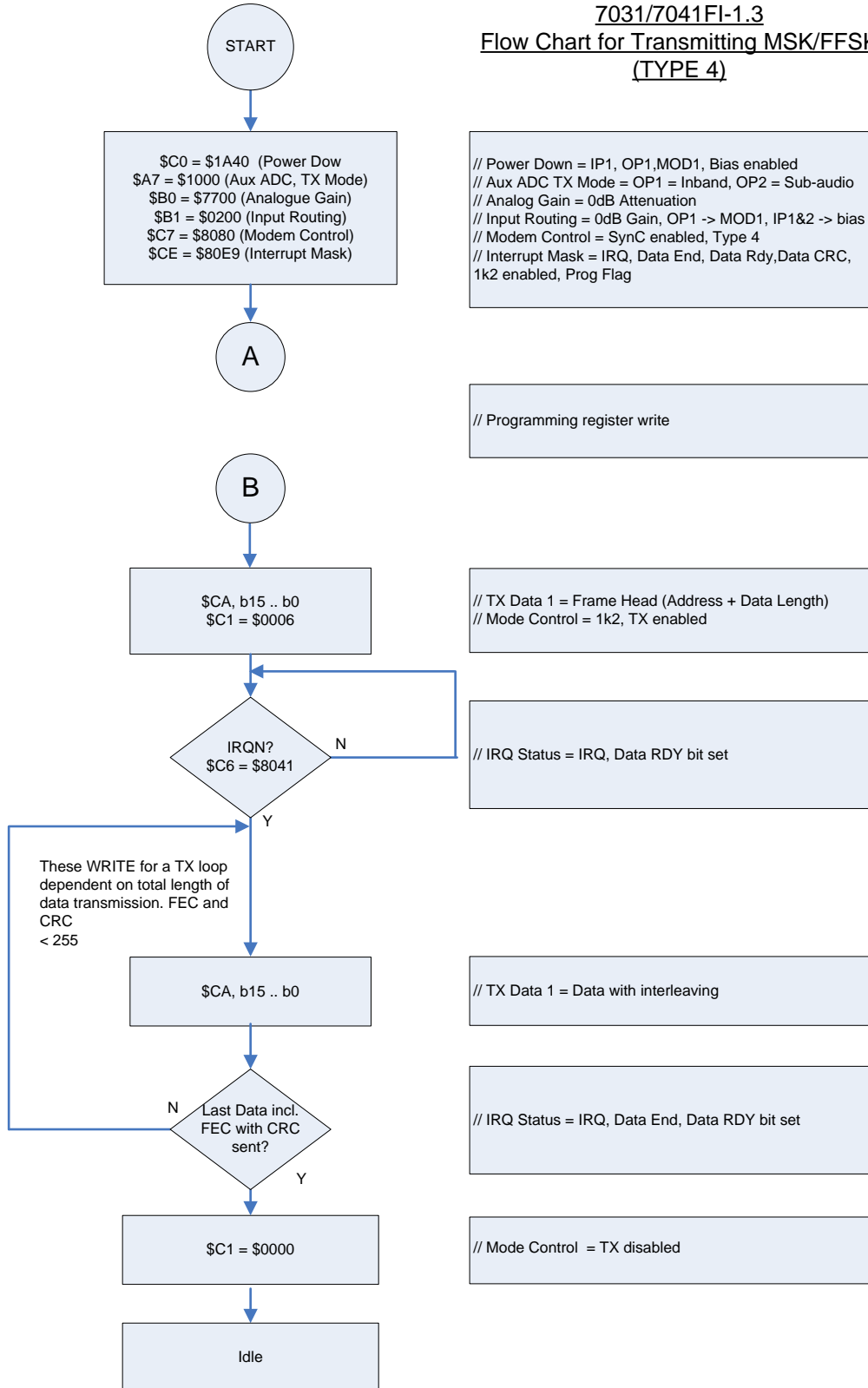
7031/7041FI-1.3
Flow Chart for Receiving MSK/FFSK
(TYPE 3)



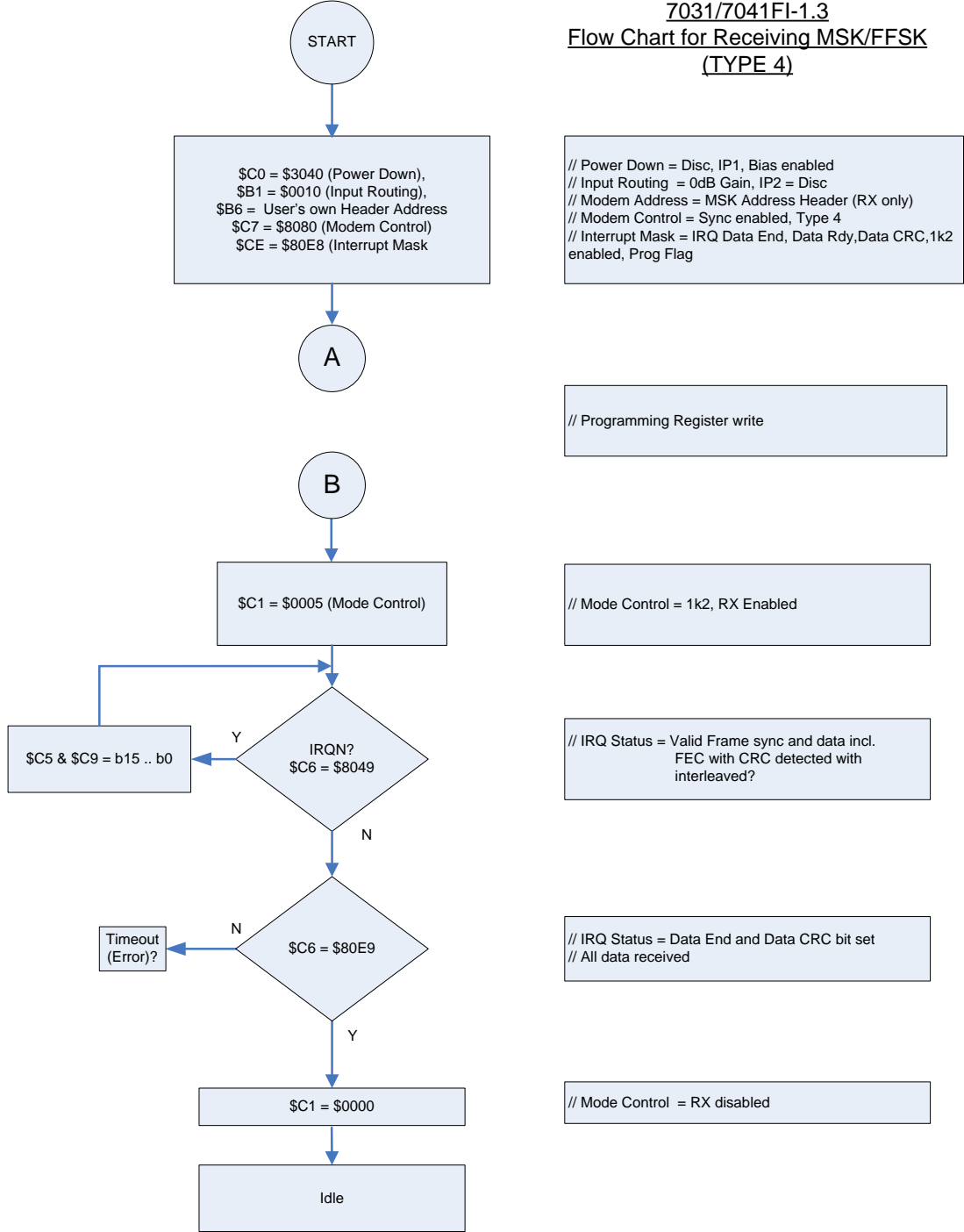
Type 4 data format



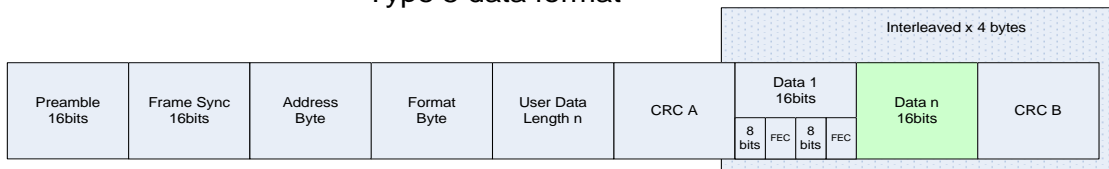
7031/7041FI-1.3 Flow Chart for Transmitting MSK/FSK (TYPE 4)



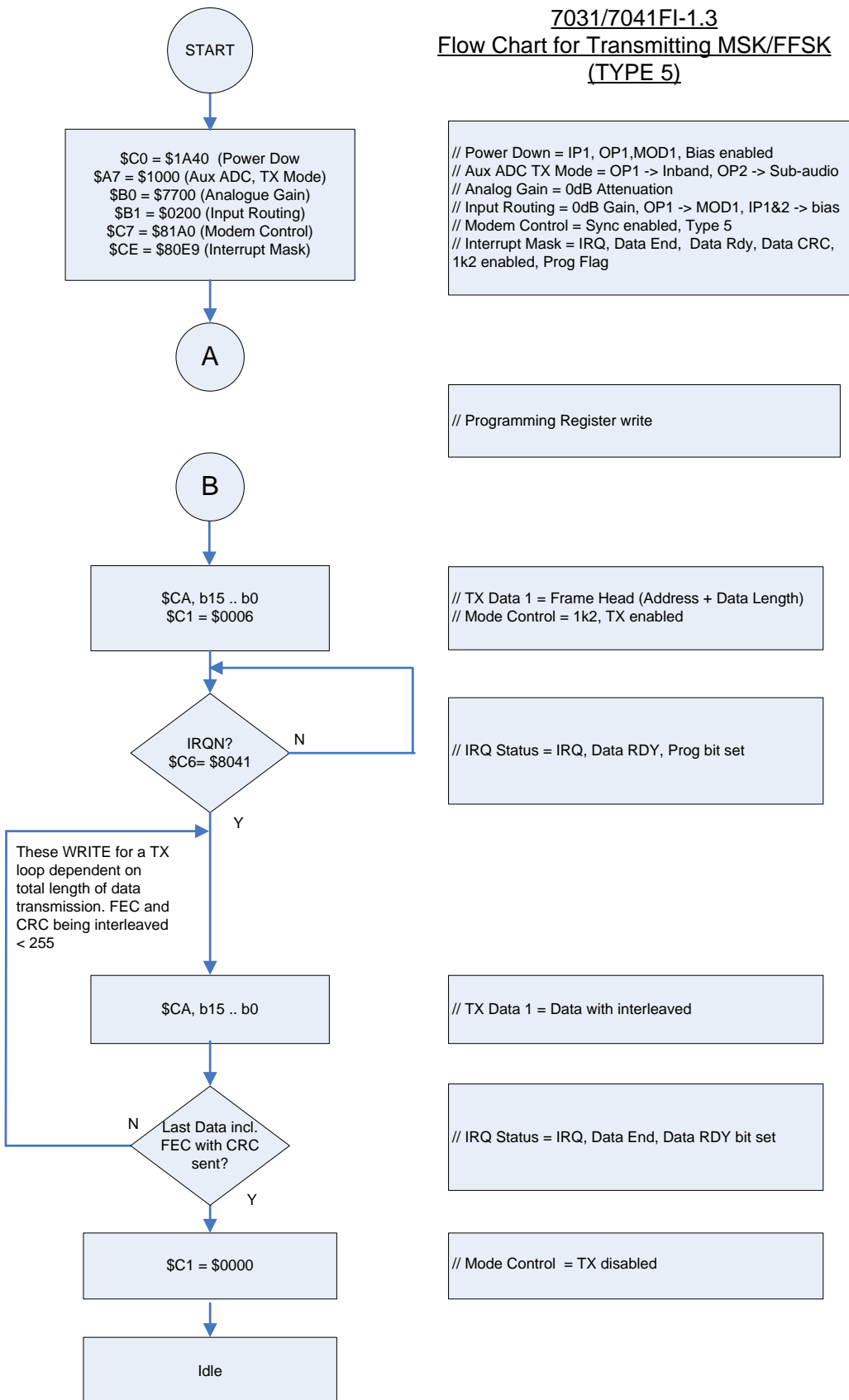
7031/7041FI-1.3
Flow Chart for Receiving MSK/FFSK
(TYPE 4)



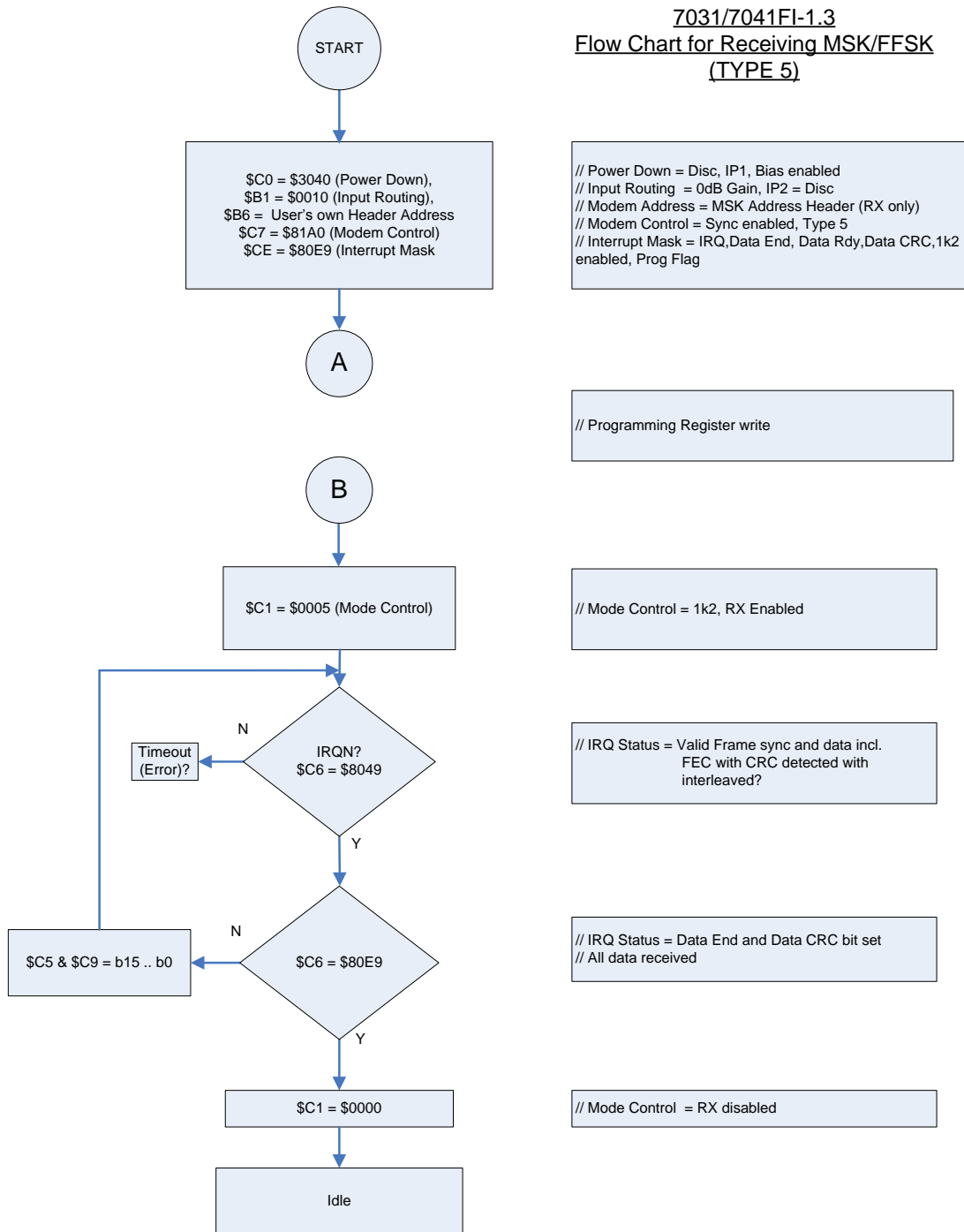
Type 5 data format



7031/7041FI-1.3 Flow Chart for Transmitting MSK/FFSK (TYPE 5)



7031/7041FI-1.3
Flow Chart for Receiving MSK/FFSK
(TYPE 5)



// Power Down = Disc, IP1, Bias enabled
 // Input Routing = 0dB Gain, IP2 = Disc
 // Modem Address = MSK Address Header (RX only)
 // Modem Control = Sync enabled, Type 5
 // Interrupt Mask = IRQ,Data End, Data Rdy,Data CRC,1k2 enabled, Prog Flag

// Programming Register write

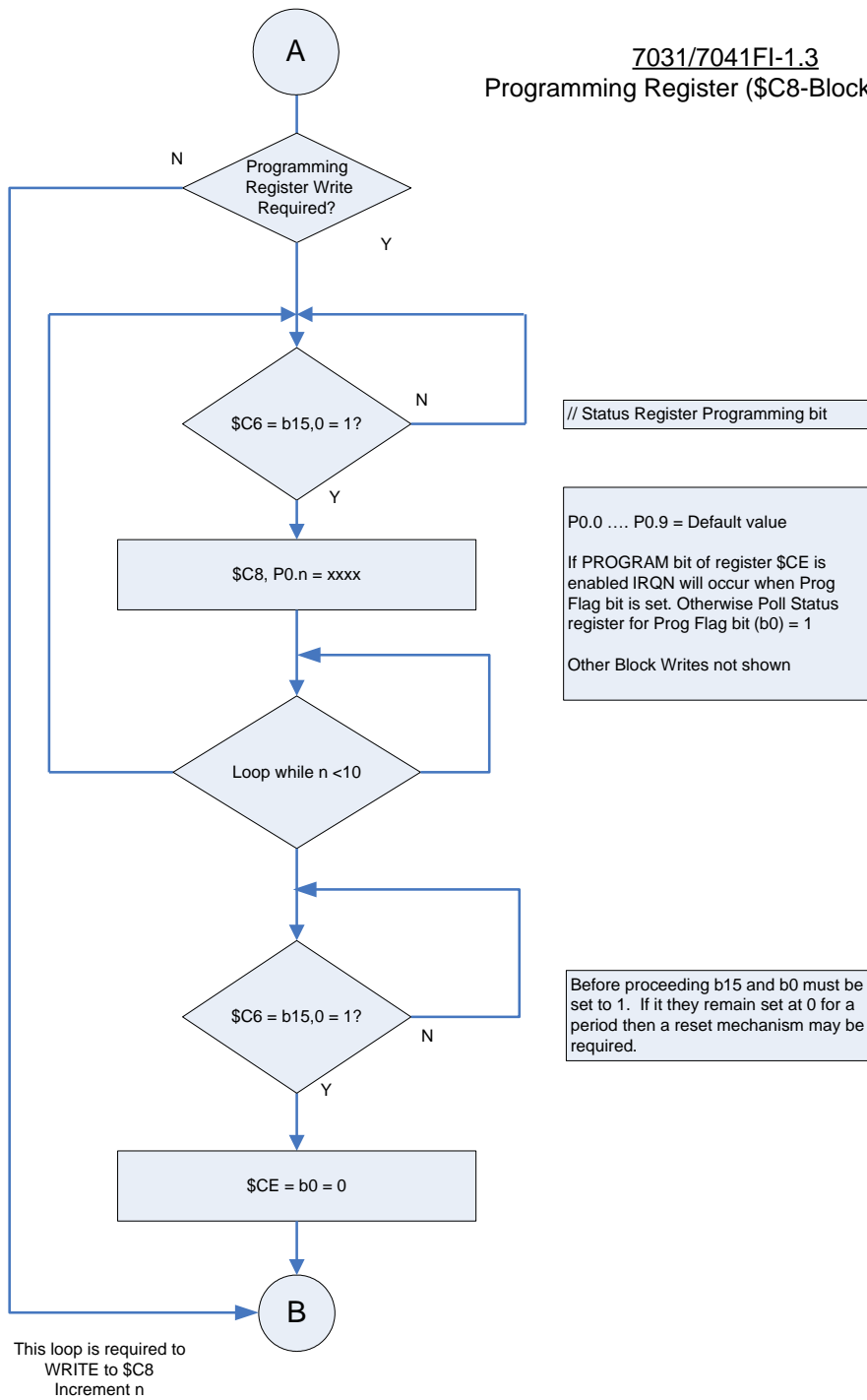
// Mode Control = 1k2, RX Enabled

// IRQ Status = Valid Frame sync and data incl.
 FEC with CRC detected with interleaved?

// IRQ Status = Data End and Data CRC bit set
 // All data received

// Mode Control = RX disabled

7031/7041FI-1.3
 Programming Register (\$C8-Block 0) Write



Note: The above diagram shows programming writes to block 0, writes to other blocks can be performed using the same method with higher values of n