CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX993/CMX993W
30MHz – 1GHz Quadrature Modulator

D/993/10 February 2013 Provisional Issue

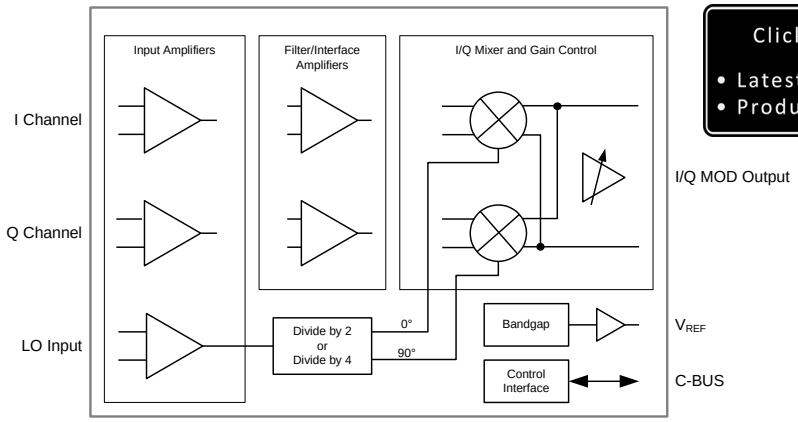
This document describes two separate, high performance, RF quadrature modulator ICs: The standard CMX993 and the wide bandwidth CMX993W product variant.

Features

- 30MHz to 1GHz Operating Frequency
- Wide Band Noise –148dBc/Hz
- Noise Floor –155dBm/Hz
- Programmable 30dB Output Gain Range
- +3dBm (PEP) Output Power
- Low LO Drive Requirements, -15dBm
- Uncommitted Amplifiers for Filtering and Interfacing
- CMX993W – Wide Bandwidth Version (>50MHz I/Q Bandwidth)
- C-BUS (SPI Compatible) Serial Interface
- Low Voltage 3.3V Operation
- Small 7x7mm VQFN Package (Q3)
- +25dBm Equivalent Output IP3

Applications

- APCO P25, Wireless Data
- ISM Transmitters
- Digital TV/CATV Modulators
- Wireless LAN, Wireless Local Loop
- IF or RF Modulators
- FSK, GMSK, 4FSK, C4FM
- QPSK, QAM, SSB, OFDM, Multi-carrier Systems
- SDR (Software Defined Radios)
- WiMAX Systems
- OFDM/COFDM Systems
- Satellite Communications
- Cellular Picocell / Nanocell Systems
- RF Channel Bandwidths up to 100MHz



1 Brief Description

The CMX993 and CMX993W are integrated, low voltage quadrature (I/Q) modulator ICs suitable for use in applications operating from 30MHz to 1000MHz. The devices integrate two matched double balanced mixers driven from a buffered and quadrature split local oscillator. The LO frequency is divided by either 2 or 4. The mixers form an I/Q vector modulator with programmable gain stages offering up to 30dB of gain, controlled in 2.5dB steps.

Uncommitted low frequency differential amplifiers are provided for users to configure. These may be used to implement functions such as filtering, differential- to single-ended signal conversion and level shifting. The CMX993W product variant offers wide-bandwidth operation.

A digital control interface, C-BUS, (an SPI compatible interface) allows gain control as well as power management of individual internal blocks to optimise system performance. The C-BUS interface operates from its own supply domain enabling the device to be interfaced to different voltage baseband devices.

The CMX993 and CMX993W devices are supplied in RF optimised VQFN packages.

CONTENTS

1.1 History

Version	Changes	Date
10	• LO input level specified to -20dBm for operation above 200MHz. • Editorial corrections	13/2/13
9	• Extra information on third order intermodulation added. • Note added for clarification in Figure 4 / Figure 4a.	13/3/10
8	• Added note 32 to AC Parameters section, identifying a drop in gain and output power below a frequency of 100MHz - typically 4dB down at 30MHz.	3/2/10
7	• Differential Amplifier connections in Figure 4 and Figure 4a corrected. • Operating characteristics clarified for Tamb rather than Tcase and at 25degC only for notes 0 and 1. • Current consumption specification reduced, following test of several wafer batches.	20/1/10
6	• Editorial corrections, Modulator Common Mode input range minimum now 1.3V and Input/Filter Amplifiers 'Input Offset' specification updated.	30/11/09
5	• Updated inline with abbreviations and pin assignments document	30/06/09
4	• CMX993W wide-bandwidth product variant included	29/05/09
3	• Lowest operating frequency specified as 30MHz	28/05/09
2	• Change to pin out and Signal List	7/11/08
1	• Original document, first approved.	14/8/08

2 Block Diagrams

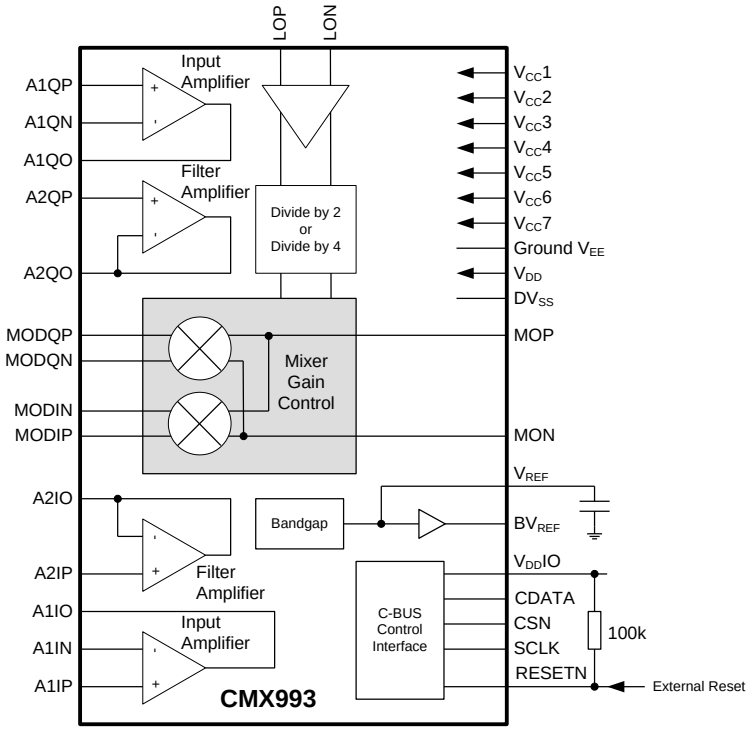


Figure 1 CMX993 Block Diagram

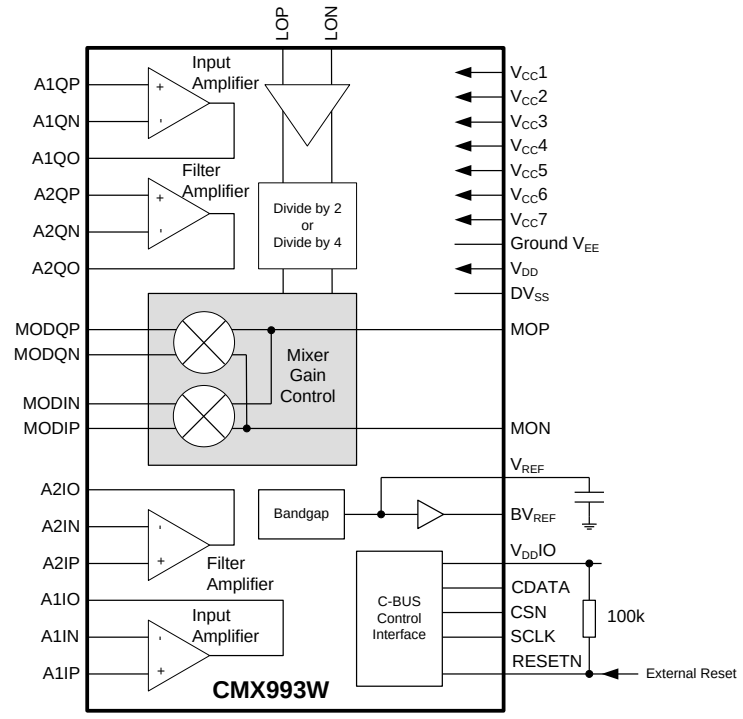


Figure 1a CMX993W Block Diagram

3 Signal List

CMX993 Pin No.	CMX993W Pin No.	Name	Signal Type	Description
-	1	A2QN	I/P	Amplifier 2 negative input (Q channel)
1	2	A2QO	O/P	Amplifier 2 output (Q channel)
2	-	NC	NC	*reserved*, do not connect to this pin
3	3	MODQP	I/P	Modulator input (Q channel)
4	4	MODQN	I/P	Modulator input reference (Q channel)
5	5	NC	NC	*reserved*, do not connect to this pin
6	6	MON	O/P	Modulator negative output
7	7	MOP	O/P	Modulator positive output
8	8	NC	NC	*reserved*, do not connect to this pin
9	9	MODIN	I/P	Modulator input reference (I channel)
10	10	MODIP	I/P	Modulator input (I channel)
11	-	NC	NC	*reserved*, do not connect to this pin
12	11	A2IO	O/P	Amplifier 2 output (I channel)
-	12	A2IN	I/P	Amplifier 2 negative input (I channel)
13	13	A2IP	I/P	Amplifier 2 positive input (I channel)
14	14	A1IO	O/P	Amplifier 1 output (I channel)
15	15	A1IN	I/P	Amplifier 1 negative input (I channel)
16	16	A1IP	I/P	Amplifier 1 positive input (I channel)
17	17	VCC1	Power	Analogue supply
18	18	VCC2	Power	Analogue supply
19	19	LON	I/P	Local Oscillator Negative Input (Note: when differentially driving LOP and LON this LON pin requires a low impedance dc path to ground otherwise it may be decoupled to ground)
20	20	LOP	I/P	Local Oscillator Positive Input (Note: this pin requires a low impedance dc path to ground)
21	21	VCC3	Power	Analogue supply
22	22	VCC4	Power	Analogue supply
23	23	VREF	O/P	Bandgap reference decoupling
24	24	BVREF	O/P	Buffered V_{REF}
25	25	NC	NC	*reserved*, do not connect to this pin
26	26	NC	NC	*reserved*, do not connect to this pin
27	27	NC	NC	*reserved*, do not connect to this pin
28	28	NC	NC	*reserved*, do not connect to this pin
29	29	VCC5	Power	Analogue supply
30	30	NC	NC	*reserved*, do not connect to this pin
31	31	NC	NC	*reserved*, do not connect to this pin
32	32	VCC6	Power	Analogue supply
33	33	NC	NC	*reserved*, do not connect to this pin
34	34	NC	NC	*reserved*, do not connect to this pin

CMX993 Pin No.	CMX993W Pin No.	Name	Signal Type	Description
35	35	NC	NC	*reserved*, do not connect to this pin
36	36	NC	NC	*reserved*, do not connect to this pin
37	37	VDD	Power	Digital supply
38	38	VDDIO	Power	Supply voltage for digital control interface
39	39	SCLK	I/P	C-BUS serial clock
40	40	CDATA	I/P	C-BUS command data input
41	41	CSN	I/P	C-BUS enable
42	42	RESETN	I/P	General reset (Reset when pin is held LOW)
43	43	DVSS	Power	Digital ground (0V)
44	44	VCC7	Power	Analogue supply
45	45	A1QP	I/P	Amplifier 1 positive input (Q channel)
46	46	A1QN	I/P	Amplifier 1 negative input (Q channel)
47	47	A1QO	O/P	Amplifier 1 Output (Q Channel)
48	48	A2QP	I/P	Amplifier 2 positive input (Q channel)
EXPOSED METAL PAD	EXPOSED METAL PAD	VEE	Power	This pad must be connected to analogue ground (0V)

Table 1 Pin List

I/P = Input
O/P = Output
T/S = 3-state
NC = reserved, do not connect to this pin

3.1 Signal Definitions

Signal Name	Pins	Usage
AV_{DD}	VCC1, VCC2, VCC3, VCC4, VCC5, VCC6, VCC7	Power supply for analogue circuits
DV_{DD}	VDD	Power supply for digital circuits
V_{DDIO}	VDDIO	Power supply voltage for digital interface (C-BUS and RESETN)
AV_{SS}	VEE (Metal pad)	Ground for all analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits
V_{REF}	VREF	Connection for decoupling of internal band-gap reference voltage
BV_{REF}	BVREF	Buffered version of V_{REF} which may be used for bias of input signals etc.

Table 2 Definition of Power Supply and Reference Voltages

4 External Components

4.1 Power Supply Decoupling

The CMX993/CMX993W has separate supply pins for the analogue and digital circuitry; a 3.3V nominal supply is recommended for all circuits but a different voltage for V_{DDIO} may be used (see section 5.4).

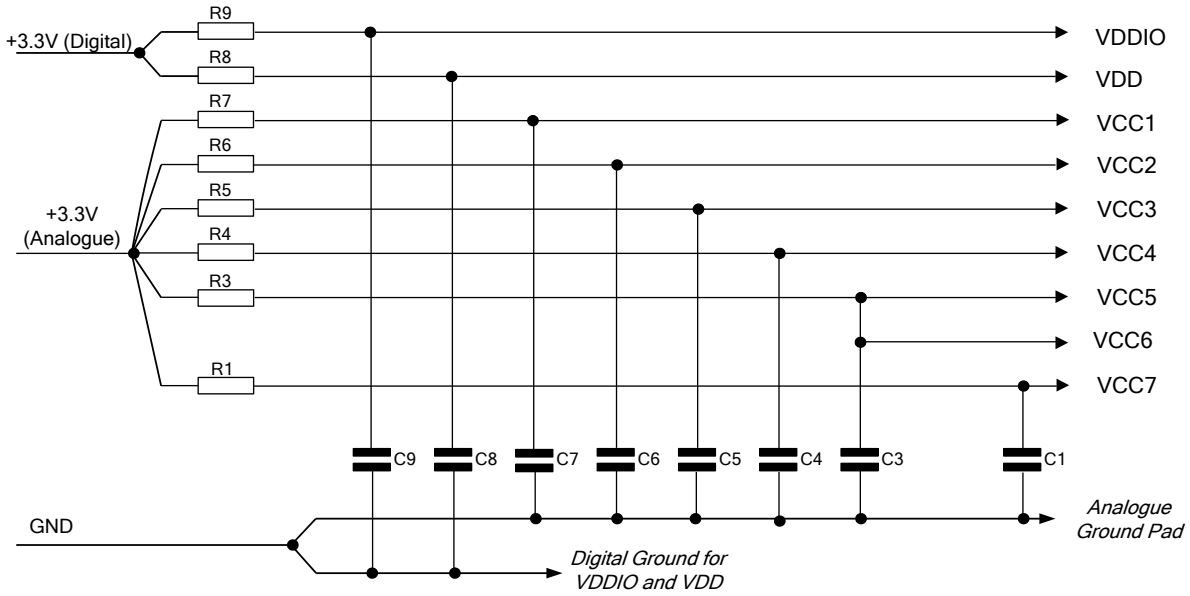


Figure 2 Power Supply Connections and Decoupling

C1	10nF	R1	3.3Ω
C3	10nF	R3	10Ω
C4	10nF	R4	3.3Ω
C5	10nF	R5	3.3Ω
C6	10nF	R6	3.3Ω
C7	10nF	R7	3.3Ω
C8	10nF	R8	10Ω
C9	10nF	R9	100Ω

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated

Note:

It is expected that low frequency interference on the 3.3V supply will be removed by active regulation; a large capacitor is an alternative but may require more board space and so may not be preferred. It is particularly important to ensure that there is no interference from V_{DDIO} (which supplies the digital I/O) that might affect the sensitive analogue supplies, like VCC1, VCC2 etc. The supply decoupling shown is intended for RF noise suppression. It is necessary to have a small series impedance prior to the decoupling capacitor for the decoupling to work well; this may be cost effectively done with the resistor and capacitor values shown. The use of resistors results in small dc voltage drops (up to approx 0.1V). Choosing resistor values approximately inversely proportional to the dc current requirements of each supply ensures the dc voltage drop on each supply is reasonably matched. In any case, the dc voltage change that results is well within the design tolerance of the device. If higher impedance resistors are used then greater care will be needed to ensure the supply voltages are maintained within tolerance, including when parts of the device are enabled or disabled.

4.2 Quadrature Modulator

Typical values for the quadrature modulator output circuits are shown in Figure 3/Table 3 and typical configuration and values for the input circuits in Figure 4/4a and Table 4. Concerning Figure 3, the transformer T1 should be located close to the CMX993/CMX993W and tracks from the MOP and MON pins to T1 should be as close to equal in length as possible, preferably with a symmetrical layout. The decoupling capacitor (C1) should be close to the centre tap of T1.

Note: Details of a simpler alternative output configuration are provided in an Application Note available from www.cmlmicro.com.

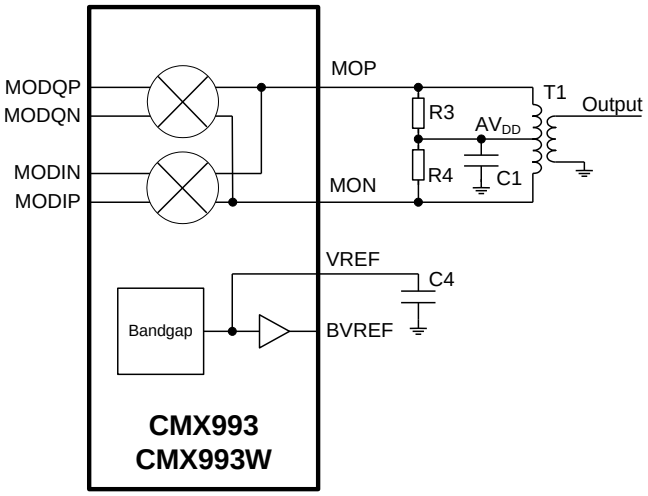


Figure 3 Modulator Output External Components (30MHz to 1GHz)

C1	10nF	T1	Balun 4:1 (See Note 1)
C4	1µF	R3, R4	(See Note 2)

Note 1: For example TC4-14+ from mini circuits; for applications between 200MHz and 1GHz or Coilcraft WBC4-1WL for applications between 30MHz and 300MHz.

Note 2: The resistors R3 and R4 are optional. Fitting these with 110Ω resistors will give a good broadband match however will reduce output level available. For many applications they will be unnecessary.

Table 3 Quadrature Modulator Output Components

The input configuration in Figure 4/4a is a possible solution for a single ended input with 0V dc bias. The input amplifiers are used to translate the input to BV_{REF}. In order to balance the small bias current drawn by the modulator, the filter amplifiers are used to buffer BV_{REF}. RC filters are used on the input to the modulator to remove wideband noise generated by the differential amplifiers. The values of the resistors and capacitors should be selected based on the bandwidths of the modulation. It is important to keep the values of R6, R7, R8 and R9 the same so that small dc offsets generated by the modulator input bias currents are matched, thereby providing the best carrier rejection. The networks R6/C1, R7/C2, R8/C3 and R9/C4 should be placed close to the modulator input pins of the CMX993/CMX993W to ensure optimum noise performance. It is important to note that due to small input bias currents, offset voltages and component tolerances it is impractical to expect this type of input configuration to give ideal carrier suppression. To achieve optimal carrier suppression it is recommended to have the ability to finely adjust the dc offsets (see section 5.1.1).

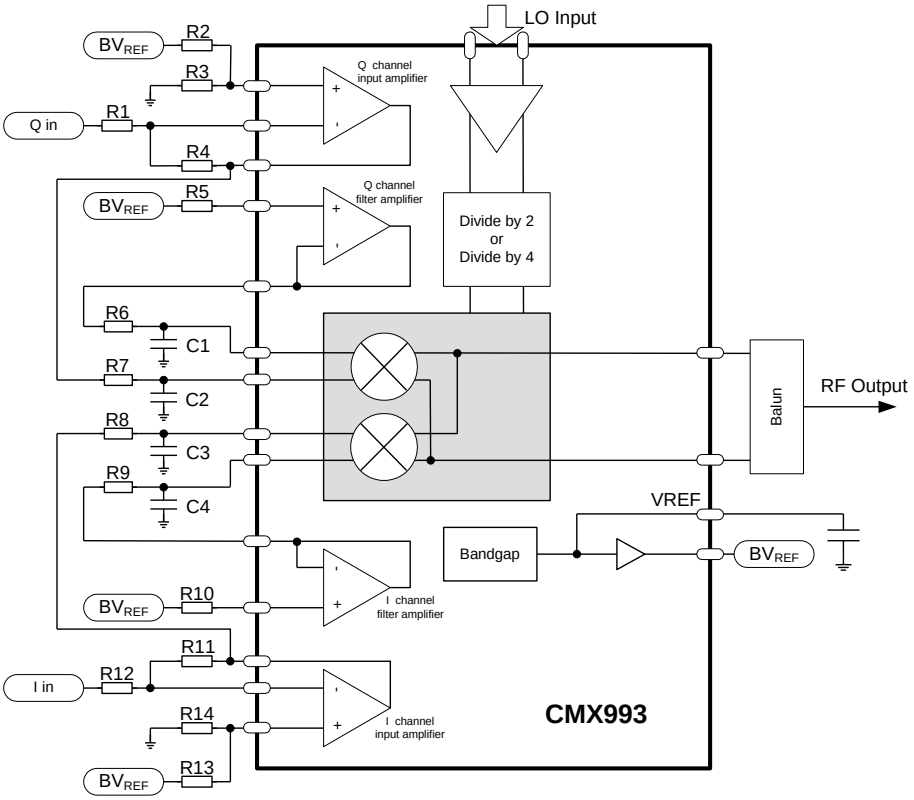
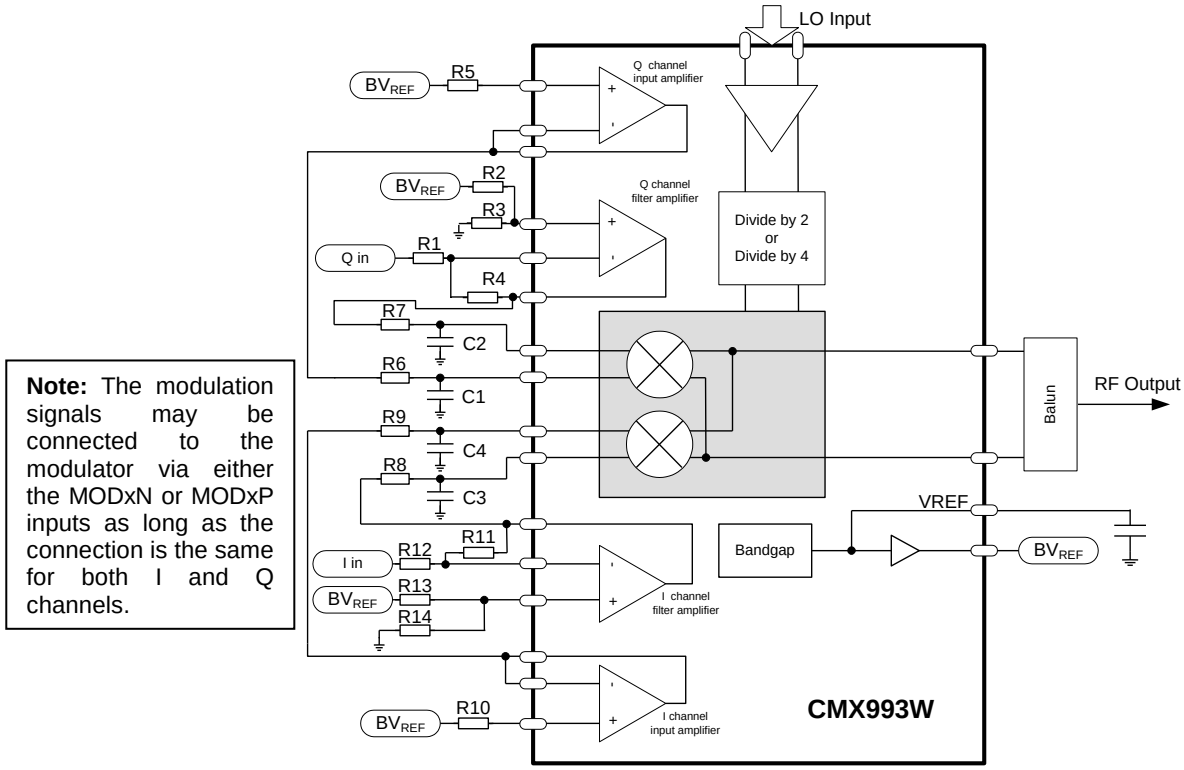


Figure 4 CMX993 Modulator and Input/Filter Amplifier Typical Configuration



Note: The modulation signals may be connected to the modulator via either the MODxN or MODxP inputs as long as the connection is the same for both I and Q channels.

Figure 4a CMX993W Modulator and Input/Filter Amplifier Typical Configuration

C1	33nF	R6	10Ω
C2	Note 1	R7	10Ω
C3	Note 1	R8	10 Ω
C4	33nF	R9	10Ω
C5	1μF	R10	5.1kΩ
R1	10kΩ	R11	5.1kΩ
R2	5.1kΩ	R12	10 kΩ
R3	10kΩ	R13	5.1kΩ
R4	5.1kΩ	R14	10kΩ
R5	5.1kΩ		

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated

Note1: Value should be selected depending on modulation bandwidth:
33nF typically for CMX993, 3.3nF typically for CMX993W

Table 4 Quadrature Modulator and Input Circuits: Typical Components

4.3 Local Oscillator Input

A 1:1 balun transformer should be used on the local oscillator input for optimum performance. In the local-oscillator divide by 4 mode, a single ended input may be used by decoupling the LON pin to ground and applying the LO signal to LOP noting that a dc path to ground on LOP must still be provided.

The divide by 4 mode is not recommended for operation below 200MHz LO frequency (50MHz RF output). For output frequencies below 50MHz the divide by 2 mode is recommended.

Users should be aware that the presence of high levels of harmonics in the signal applied to the LO Input might degrade quadrature accuracy.

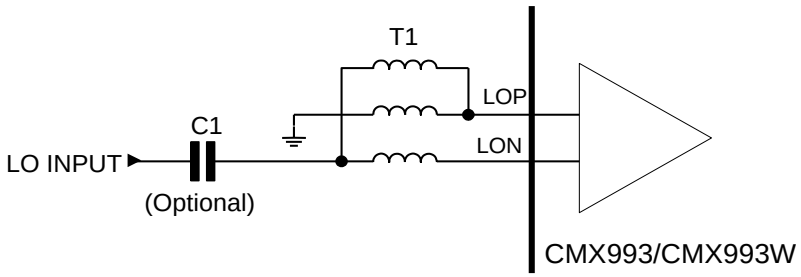


Figure 5 LO Input Configuration using a 1:1 Balun (60MHz to 2GHz)

C1	1nF	T1	Balun 1:1 (e.g. MABA-007748-CT11160) from M/A-com, see Note 3)

Notes:

1. The configuration of the 1:1 balun used at the LO input has to create a dc path to analogue GND for both LO inputs, LOP and LON as shown in Figure 5.
2. The capacitor C1 is optional and should be used where the 0V dc connection provided by the balun is not acceptable to the circuitry providing the LO signal.
3. The MABA-007748-CT11160 is specified between 5MHz and 1.2GHz. The part has been found to remain functional with the CMX993/CX993W up to at least 2GHz however such operation is outside the manufacturer's rating.

5 General Description

The CMX993 and CMX993W are RF quadrature modulators with additional features such as gain control and uncommitted differential amplifiers. Detailed block diagrams for the ICs are shown in section 2. The ICs can support a wide range of modulation formats and standards including TDMA operation.

The following sections describe the functionality of the ICs.

5.1 Quadrature Modulator

The quadrature modulator provides translation from baseband I and Q signals to a modulated RF signal. The wideband inputs can be driven differentially or single-ended. In the case of single ended operation a reference voltage equal to the nominal dc level of the modulation must be supplied. The input and filter amplifiers allow single-ended signals to be translated to an appropriate dc level, one solution for an input signal with 0V dc bias is shown in Figure 4/4a.

5.1.1 DC Offsets and Carrier Leakage

The modulator inputs (MODIN/MODIP and MODQN/MODQP) are differential and require a common dc level or common mode voltage. Differences in the bias voltages on the pins will result in an increased level of carrier present at the output. Care should be taken to minimise offsets, thereby minimising carrier leakage.

Some systems implement carrier nulling before transmission. This results in a compensation of the small internal offsets in the modulator and any offsets generated in external circuits. Digital to analogue converters designed for I/Q systems, e.g. CMX981, often include registers which allow a programmable offset to be applied to the I/Q signals, making this nulling process straightforward.

5.1.2 Wideband Noise and Gain Control

The wideband noise of this modulator is optimised to ensure a low noise floor at the output, compliant with common product standards. This stage also provides gain control, which allows the output level to be adjusted while maintaining the maximum possible signal-to-noise ratio.

To ensure optimum performance the I/Q input signals need to be free from noise. The input bandwidth of the modulators is quite broad, so any noise on the I/Q signals will get translated to the RF output. Such noise can generally be removed by simple RC filters, as shown in Figure 4/4a. Careful attention needs to be paid to the bandwidth of these filters as, if unduly narrow, they can affect the modulation, degrading image rejection and modulation accuracy.

5.2 Differential Amplifiers

5.2.1 Input Amplifiers

Two differential amplifiers are provided which may be used for signal conditioning, for example conversion of differential input signals to single ended format, or to provide dc level translation. The amplifiers are uncommitted, with the differential inputs and the output all available on pins. The stages are low power and are enabled using the ‘General Control Register’ (see section 6.2). It is not possible to independently control each amplifier, both are enabled with a common control bit.

5.2.2 Filter Amplifiers

A further pair of amplifiers are provided which may be used to implement filtering or buffering. These uncommitted amplifiers (configured as voltage followers in the case of the CMX993) may be used to implement Sallen-Key style filters or configured as needed.
The amplifiers are low power and are enabled using the 'General Control Register' (see section 6.2). It is not possible to independently control each amplifier, both are enabled with a common control bit.
Note: Input Amplifiers and Filter Amplifiers have independent controls.

5.2.3 CMX993/CMX993W Difference

The essential difference between the CMX993 and the CMX993W is the amplifier stage provided for the Filter Amplifier. In the CMX993, the Input Amplifier and Filter Amplifier are of a similar design with a gain-bandwidth product of about 10MHz. To support wider modulation bandwidths the CMX993W uses a high-speed amplifier for the Filter Amplifier (Note: only the Filter Amplifier is different, the Input Amplifier in the CMX993W is the same as the Input amplifier in the CMX993.) Because of the extra gain/bandwidth in the CMX993W a 'gain reduction' mode is provided for the CMX993W Filter Amplifier, see section 6.2.

5.3 Reference Voltages

The CMX993/CMX993W includes on-chip reference voltage generation. Any noise present on the VREF pin should be decoupled to Analogue Ground (V_{EE}). A buffered version of the reference is provided on the BVREF pin. After further filtering to remove noise, this may be used to provide the dc reference for modulator mixer inputs.

5.4 Data Interface

The CMX993/CMX993W is controlled via a three wire C-BUS. A further pin (RESETN) is provided which, when 'low', generates a reset signal (see section 6 for further details). This pin should be pulled to V_{DDIO} with a suitable resistor (e.g. 100kΩ) if not used.

The data interface can run at a lower voltage than the rest of the IC by setting V_{DDIO} to the required interface level in the range 1.6V to 3.6V. Full details of the control register structure are given in section 6.

6 C-BUS Interface and Register Description

This block provides for the transfer of data and control information between the CMX993/CMX993W internal registers and the µC over the C-BUS serial bus. Each transaction consists of a single Register Address byte sent from the µC which may be followed by one Data byte sent from the µC, to be written into one of the CMX993/CMX993W registers, as illustrated in Figure 9.

Data sent from the µC on the CDATA line is clocked into the CMX993/CMX993W on the rising edge of the SCLK input. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine. Figure 9 gives detailed C-BUS timing requirements.

The following C-BUS addresses and registers are:

General Reset Register (Address only, no data)	Address $01
General Command, 8-bit write only.	Address $02
Gain Control, 8-bit write only.	Address $05
Frequency Control Register, 8-bit write only	Address $08

Notes:

- All registers will retain data if V_{DD} and V_{DDIO} are held high, even if all other power supply pins are disconnected.
- If clock and data lines are shared with other devices V_{DD} and V_{DDIO} must be maintained in their normal operating ranges otherwise ESD protection diodes may cause a problem with loading signals connected to SCLK and CDATA pins, preventing correct programming of other devices. Other supplies may be turned off and all circuits on the IC may be powered down without causing this problem.

6.1 General Reset Command: C-BUS address $01

This command resets the device and clears all bits in all registers. The General Reset command places the device into powersave mode.

Whenever power is applied to the DVDD pin, a built in power-on-reset circuit ensures that the device powers-up into the same state as that following a General Reset command. The RESETN pin on the device will also reset the device into the same state.

6.2 General Control Register: C-BUS address $02 8-bit write-only

This register controls general features such as powersave.
All bits of this register are cleared to 0 by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	I/Q Pwr	0	V_{REF}	Filter Amps Pwr CMX993 only	Input Amps Pwr	Wideband Filter Amps Pwr CMX993W only	0	Filter Amp Gain Reduction CMX993W only

General Control Register b7-b1: Select high input gain
These bits control power up/power down of the various blocks of the IC. In all cases, '1' = power up, '0' = power down.

b7	Enable I/Q modulator and local oscillator sections
b6	*reserved*, set to '0'
b5	Enable internal bias circuits and bandgap reference (V_{REF} and BV_{REF}).
b4	CMX993 – Enable filter amplifiers
	CMX993W – reserved, set to '0'
b3	Enable input amplifiers
b2	CMX993 – reserved, set to '0'
	CMX993W – Enable wide bandwidth filter amplifiers
b1	*reserved*, set to '0'

General Control Register b0: Filter Amplifier Gain Reduction

b0 = 1	CMX993W – Wide bandwidth filter amplifier gain reduction by adding 1kΩ between output and negative input.
b0 = 0	CMX993W – Normal Operation
b0	CMX993 – *reserved*, set to '0'

6.3 Gain Control Register: C-BUS address $05 8-bit write-only

This register controls the gain of the I/Q modulator.

Bit:	7	6	5	4	3	2	1	0
	0	F4	F3	F2	F1	0	0	0

Gain Control Register b2-b0: Reserved for future use, set to '0'.

Gain Control Register b6-b3: Modulator Attenuation

b6	b5	b4	b3	
F4	F3	F2	F1	
1	1	0	0	30dB Attenuation
1	0	1	1	27.5dB Attenuation
1	0	1	0	25dB Attenuation
1	0	0	1	22.5dB Attenuation
1	0	0	0	20dB Attenuation
0	1	1	1	17.5dB Attenuation
0	1	1	0	15dB Attenuation
0	1	0	1	12.5dB Attenuation
0	1	0	0	10dB Attenuation
0	0	1	1	7.5dB Attenuation
0	0	1	0	5dB Attenuation
0	0	0	1	2.5dB Attenuation
0	0	0	0	0dB Attenuation (Max Gain)

Gain Control Register b7: Reserved for Modulator Attenuation, set to '0'.

6.4 Frequency Control Register: C-BUS address $08 8-bit write-only

Bit:	7	6	5	4	3	2	1	0
	0	0	0	DIV	0	0	F2	F1

Frequency Control Register b7-5 and b3-2: Reserved for future use, set to '0'.

Frequency Control Register b4: Local Oscillator Divider Control

Writing ‘b4’ = 1 will enable "divide the local oscillator by 4" mode, writing ‘b4’ = 0 will enable the "divide the local oscillator by 2" mode.

NOTE: Divide by 4 mode is not recommended for operation below 200MHz LO frequency (50MHz RF output). For output frequencies below 50MHz the divide by 2 mode is recommended.

Frequency Control Register b1-b0

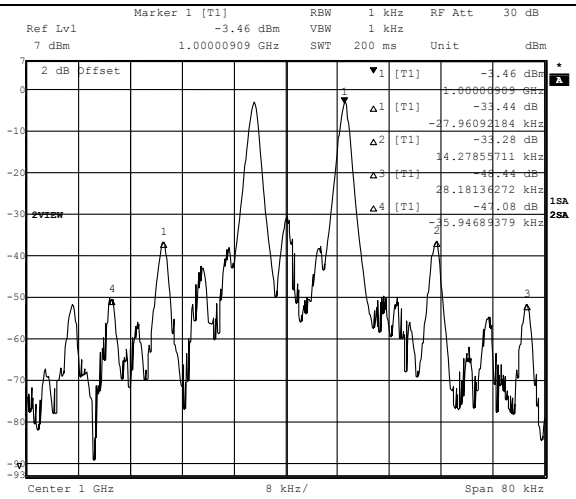
Controls the operating frequency band.

b1	b0	
F2	F1	
0	0	Operation below 500MHz
0	1	Operation above 500MHz
1	0	*reserved*
1	1	*reserved*
Note: Frequencies are the operating frequency, not the local oscillator input frequency.		

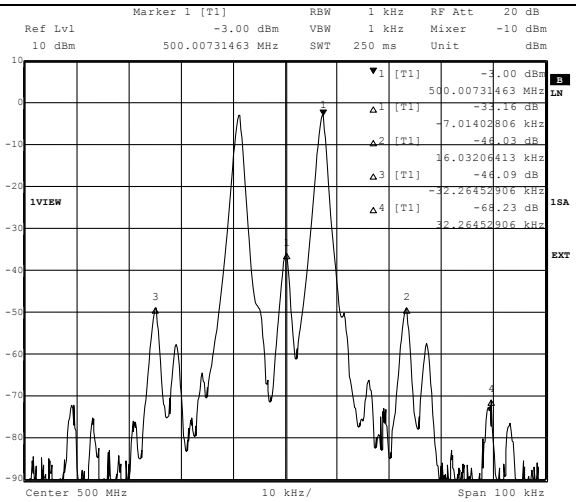
7 Application Notes

7.1 Typical Performance

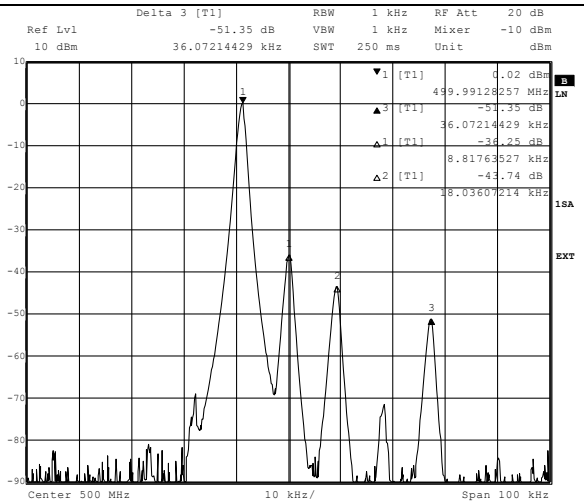
Examples of typical performance which may be achieved when using the CMX993/CMX993W are shown below.



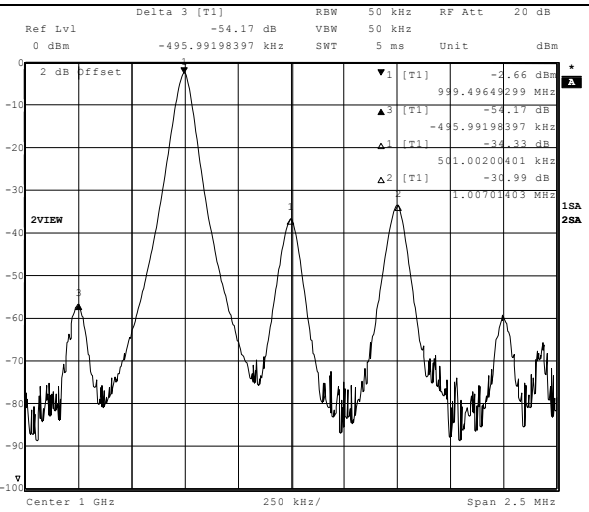
Two-tone signal at 1GHz, +3dBm PEP output, modulator driven from 'filter amp', LO = 2GHz, -15dBm.



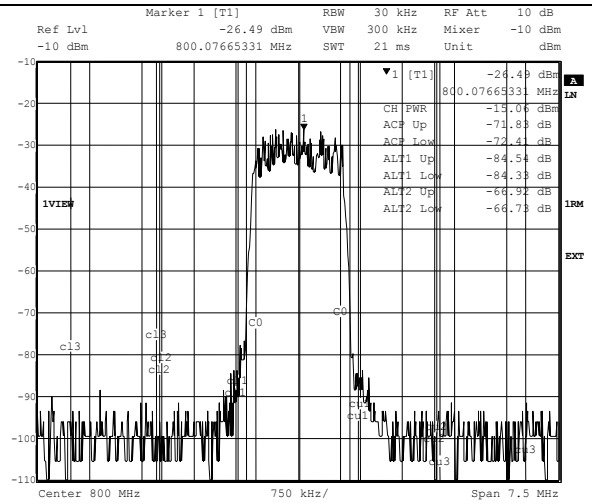
Two-tone signal at 500MHz, +3dBm PEP output, modulator driven from 'Input amp', LO = 2GHz, -15dBm.



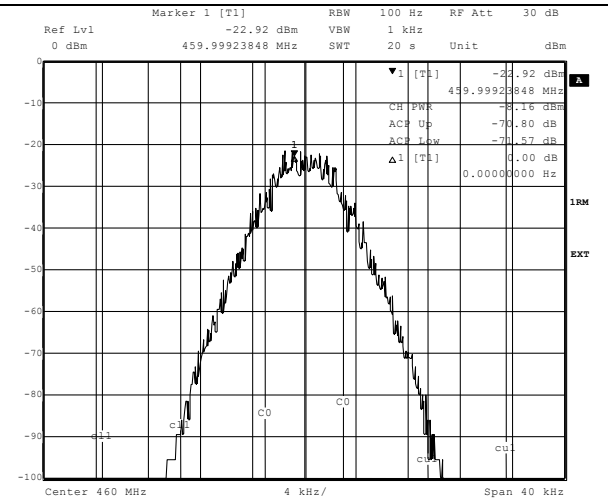
0dBm single-tone at 500MHz, modulator driven from 'Input amp', LO = 2GHz, -15dBm.



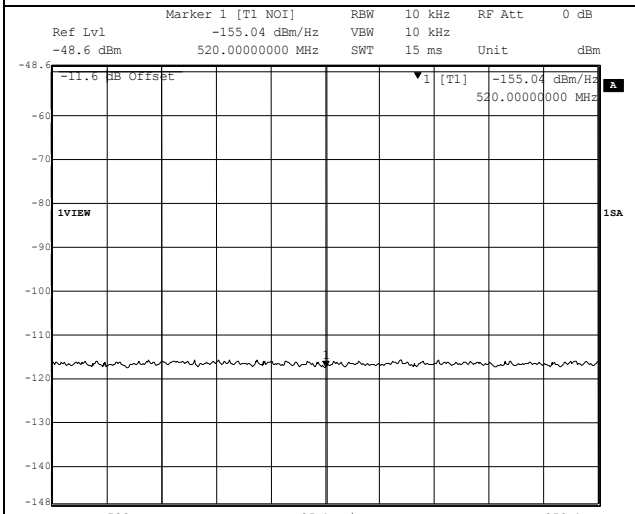
Wideband performance with single-tone (500kHz) at 1GHz, modulator driven from 'input amp', LO = 2GHz, -15dBm.



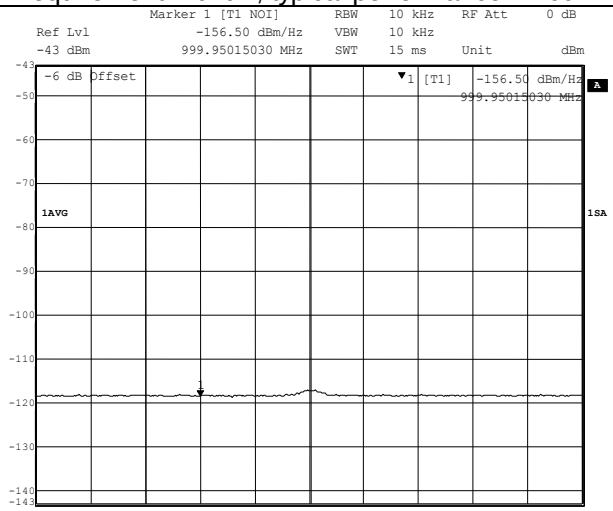
IS-95 reverse channel operation at 800MHz, measured at 885kHz, 1.98kHz and 2.65MHz



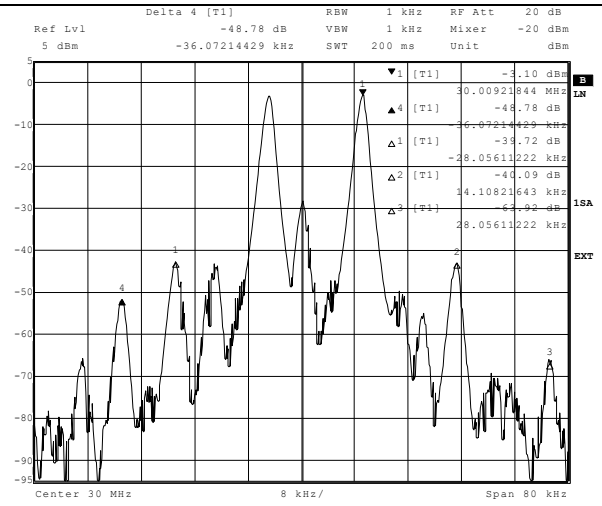
C4FM modulation for APCO Project 25 (TIA/EIA 102.BAAA); Measurement is 'non-spurious adjacent channel power ratio' (TIA/EIA 102.CAAB-B), requirement = 67dB, typical performance = 70dB



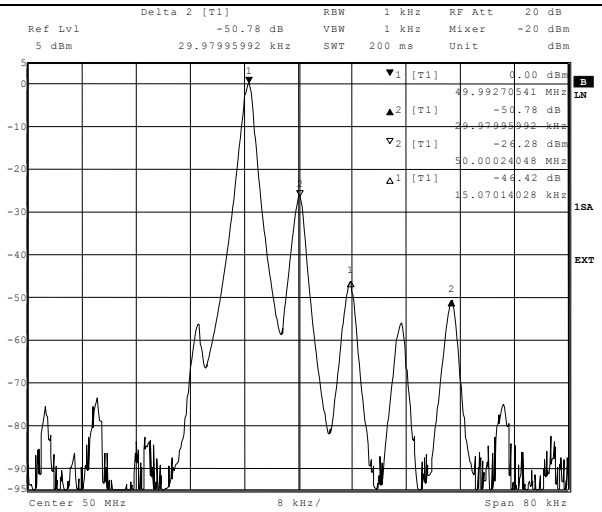
500MHz noise floor, carrier at 500MHz



1GHz noise floor, carrier at 980MHz



Two-tone signal at 30MHz, +3dBm PEP output, modulator driven from 'filter amp', LO = 60MHz, -10dBm.



0dBm single-tone at 50MHz, modulator driven from 'Input amp', LO = 100MHz, -10dBm.

7.2 Intermodulation and Modulator Spurious

When selecting an I/Q modulator for a particular application users should take care as intermodulation performance figures given in datasheets can sometimes be difficult to interpret. Some devices similar to the CMX993 quote 'output IP3' performance that is only achieved at reduced input / output levels. It has been observed that at their rated output power the performance of these devices is degraded (see Figure 6). By contrast the CMX993 output IP3 is constant when measured with different input / output levels for a given frequency. Typical 'Equivalent Output IP3' is in the range 23dBm to 25dBm at 400MHz; lower values can be expected at higher frequencies and below 100MHz.

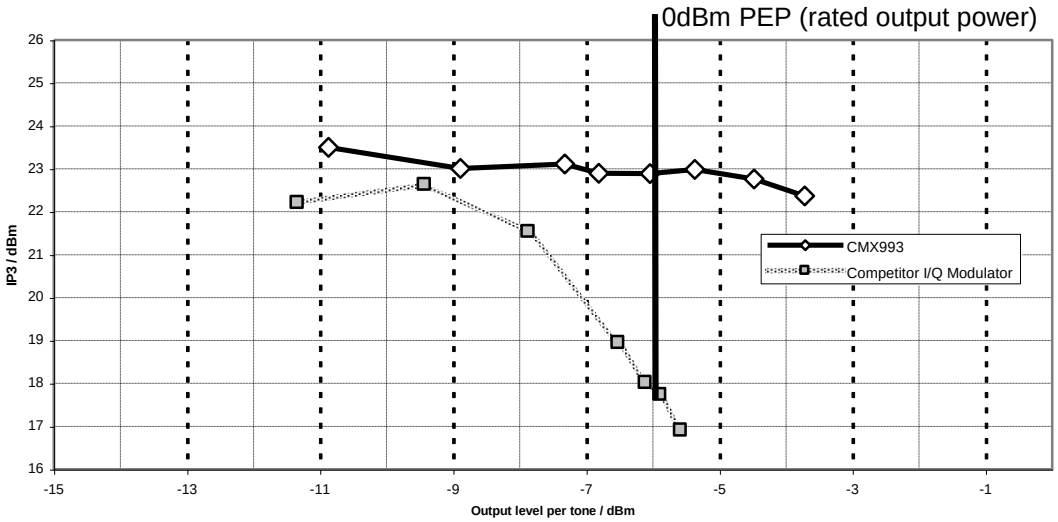


Figure 6 – Variation in Effective Equivalent IP3 with signal level

Another issue that has been observed with alternative I/Q modulator devices is that the third-order products are not always the largest distortion products. This will be observed in Figure 7 where a competitor's device exhibits larger distortion products resulting from the third harmonics of the modulation than the classic 3rd order intermodulation products. Figure 8 shows the equivalent CMX993 performance at the same output power and frequency.

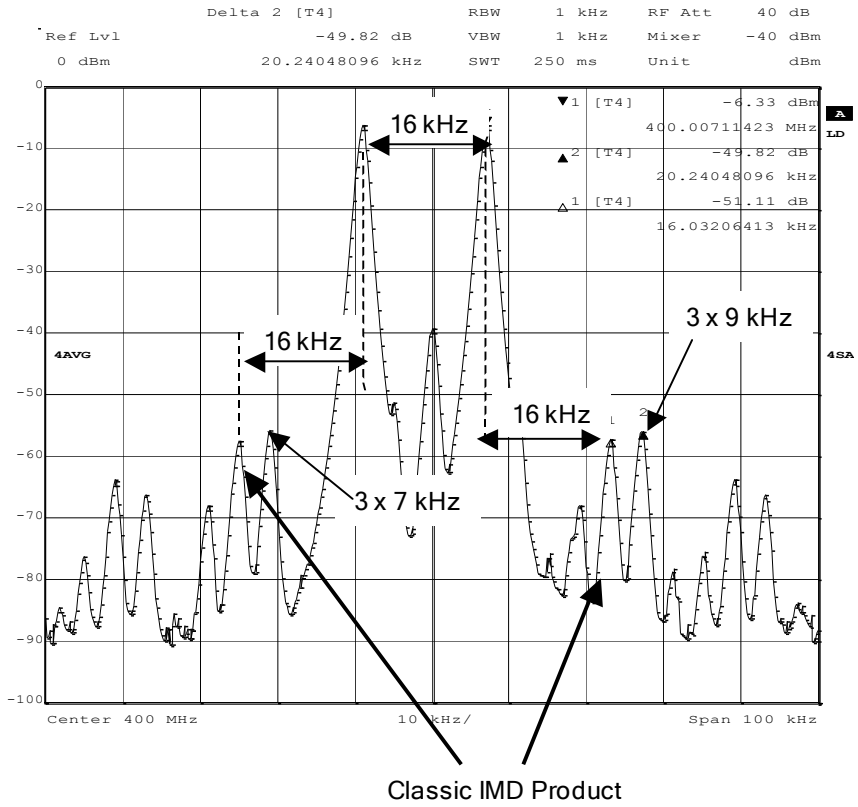


Figure 7 – IMD Performance of alternative I/Q Modulator at 0dBm PEP (7kHz and 9kHz tones)

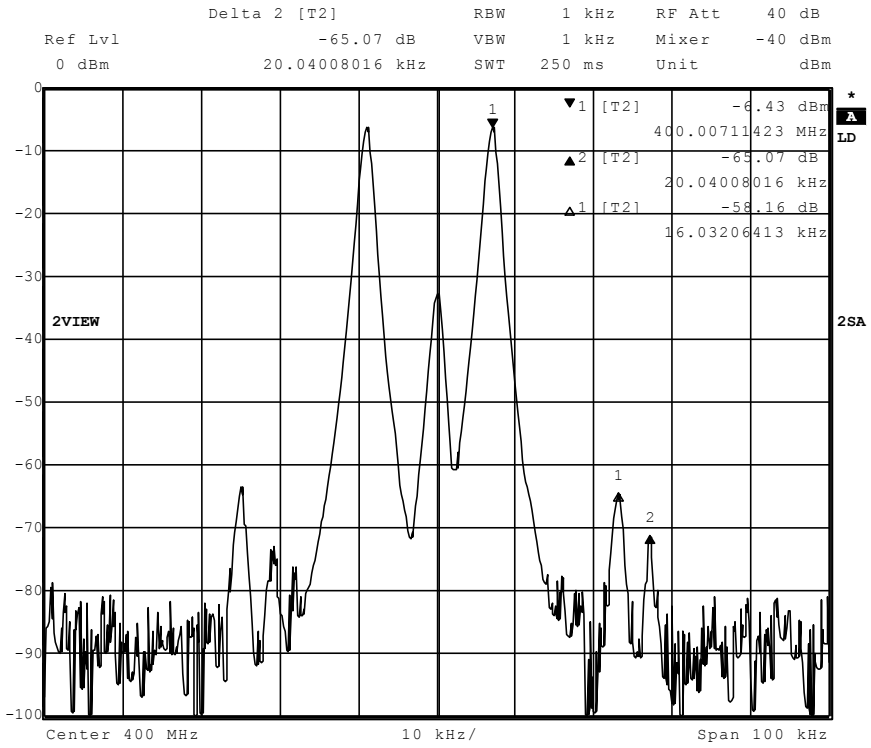


Figure 8 – IMD Performance of CMX993 at 0dBm PEP (7kHz and 9kHz tones)

8 Performance Specification

8.1 Electrical Performance

For a definition of voltage and reference signals see Table 2.

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (AV_{DD} - AV_{SS}) or (DV_{DD} - DV_{SS})	-0.3	+4.0	V
Voltage on any pin to AV_{SS} or DV_{SS}	-0.3	V_{DD} + 0.3	V
Voltage between AV_{SS} and DV_{SS}	-50	+50	mV
Current into or out of DVSS, AVDD or DVDD pins	-75	+75	mA
Current into or out of AV_{SS} (VEE, exposed metal pad)	-200	+200	mA
Current into or out of any other pin	-30	+30	mA

Q3 Package	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C	-	1750	mW
... Derating (see Note below)	-	17.5	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

Note: Junction-to-ambient thermal resistance is dependent on board layout and mounting arrangements. The derating factor stated will be better than this with good connection between the device and a ground plane or heat sink.

8.1.2 Operating Limits

	Notes	Min.	Max.	Units
Supply (AV_{DD} – AV_{SS}) and (DV_{DD} – DV_{SS})		3.0	3.6	V
IO Supply (V_{DDIO} – DV_{SS})		1.6	3.6	V
Operating Temperature (see Note above)		-40	+85	°C

8.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = AV_{DD} = DV_{DD} = 3.3V; V_{DDIO} = 1.6V to V_{DD}; V_{SS} = AV_{SS} = DV_{SS}. LO Level = -15dBm and T_{AMB} = -40ºC to +85ºC.

DC Parameters	Notes	Min.	Typ.	Max.	Units
Total Current Consumption					
Powersave mode	0	-	10	70	µA
Band gap V_{REF} only		-	50	-	µA
Operating	1	-	95	-	mA
Current from V_{DDIO}	2	-	-	600	µA
Logic '1' Input Level		70%	-	-	V_{DDIO}
Logic '0' Input Level		-	-	30%	V_{DDIO}
Logic Input Leakage Current (Vin = 0 to DV_{DD})		-1.0	-	+1.0	µA
Output Logic '1' Level (I_{OH} = 0.6 mA)		80%	-	-	V_{DDIO}
Output Logic '0' Level (I_{OL} = -1.0 mA)		-	-	+0.4	V
Power up time		-	-		
Voltage Reference	3	-	-	0.5	ms
All blocks except Voltage Reference	3	-	-	10	µs
Reference Voltage (V_{REF}, BV_{REF})		1.45	1.6	1.75	V

Notes:

0. Powersave mode includes the case after general reset with all analogue and digital supplies applied and also the case with V_{DD} applied but with all analogue supplies disconnected (i.e. in this latter scenario power from V_{DD} will not exceed the specified value, whatever the state of the registers). At T_{AMB} = 25ºC, not including any current drawn from device pins by external circuitry.
1. For CMX993 only. Add 1mA for CMX993W device. T_{AMB} = 25ºC only.
2. Assumes 30pF on each C-BUS interface line and an operating serial clock frequency of 5MHz.
3. Time from the rising edge of the last serial clock input following CSN being asserted for a write to the appropriate control register.

AC Parameters	Notes	Min.	Typ.	Max.	Units
Output Frequency Range		30	-	1000	MHz
Local oscillator input					
LO Frequency Range	4, 28	60	-	2000	MHz
LO Input Impedance (Differential)		-	50	-	Ω
LO Input Level					
200MHz < F < 2000 MHz	33	-20	-	-10	dBm
80MHz < F < 200MHz	28	-15	-	-10	dBm
60MHz < F < 80MHz	27,28	-10	-	-5	dBm
Input amplifiers (and filter amplifiers – CMX993)					
Gain Bandwidth Product	15	-	10	-	MHz
Input Offset Voltage	31	-	3	6	mV
Input Common Mode Range	17	1.0	1.6	2.5	V
Input Bias Current		-	0.4	-	µA
Input Resistance		-	160	-	kΩ
Slew Rate	15	-	6	-	V/µs
IMD	15, 16, 19	-	-85	-	dB
Differential Input Voltage	18	-	-	1.2	V
Input Referred Noise at 1kHz		-	15	-	nV/√Hz
Output Load	13	-	1kΩ ‖ 100pF	-	
DC Output Range		AV_{SS}+0.1	-	AV_{DD}-0.1	V
Filter amplifiers – CMX993W					
Gain Bandwidth Product	15	-	65	-	MHz
Input Offset Voltage	31	-	3	4	mV
Input Common Mode Range	17	1.1	1.6	2.5	V
Input Bias Current		-	1.6	4.5	µA
Input Resistance		-	38	-	kΩ
Slew Rate	15	-	32	-	V/µs
IMD	15, 16, 19	-	-90	-	dB
Differential Input Voltage	18	-	-	1.2	V
Input Referred Noise at 1kHz		-	5	-	nV/√Hz
Output Load	13	-	1kΩ ‖ 100pF	-	
DC Output Range		AV_{SS}+0.2	-	AV_{DD}-0.8	V

AC Parameters	Notes	Min.	Typ.	Max.	Units
Quadrature Modulator					
DC Bias Input	14	-	1.6	-	V
I/Q Input Common Mode Voltage		1.3	1.55	1.7	V
I/Q Mixer Input Voltage	10	-	0.5	-	Vp-p
Modulator Minimum Input Bandwidth		-	50	-	MHz
Voltage Gain	24, 32	-	-2	-	dB
Transmit Gain Control Range		-	30	-	dB
Transmit Gain Control Step Size		-	2.5	-	dB
Gain Switching Time	25	-	-	10	µs
Transmit Output Power (PEP)	5,6, 20, 32	-	+3	-	dBm
Noise Floor	25, 29	-	-155	-	dBm/Hz
Wideband Noise During Modulation	7, 8, 30	-	-148	-145	dBc/Hz
Output Noise with Attenuation Steps	9, 12, 20				
Attenuation = 5dB		-	-	-153	dBm/Hz
Attenuation = 10dB		-	-	-155	dBm/Hz
Attenuation = 15dB		-	-	-156	dBm/Hz
Attenuation = 20dB		-	-	-158	dBm/Hz
Attenuation = 25dB		-	-	-159	dBm/Hz
Image Suppression				-	
At 30MHz		-	32	-	dB
At 100MHz		-	40	-	dB
At 500MHz		TBD	40	-	dB
At 1GHz		TBD	32	-	dB
Carrier Suppression	23	-35	-40	-	dBm
Intermodulation	11	30	-	-	dB
Equivalent Output IP3		-	25	-	dBm
IS-95 Performance	26				
1st Adjacent Channel (Δf=885kHz)		-	-72	-	dB
2nd Adjacent Channel (Δf=1.98MHz)		-	-84	-	dB
3rd Adjacent Channel (Δf=2.65MHz)		-	-67	-	dB
1dB Compression Point	29	-	+8	-	dBm
Load Impedance (Differential)	21	-	100	-	Ω
Discrete Unwanted Emissions (other than harmonics of the output) in the Frequency Range 9kHz –12.75 GHz.	22	-	-	-80	dBc

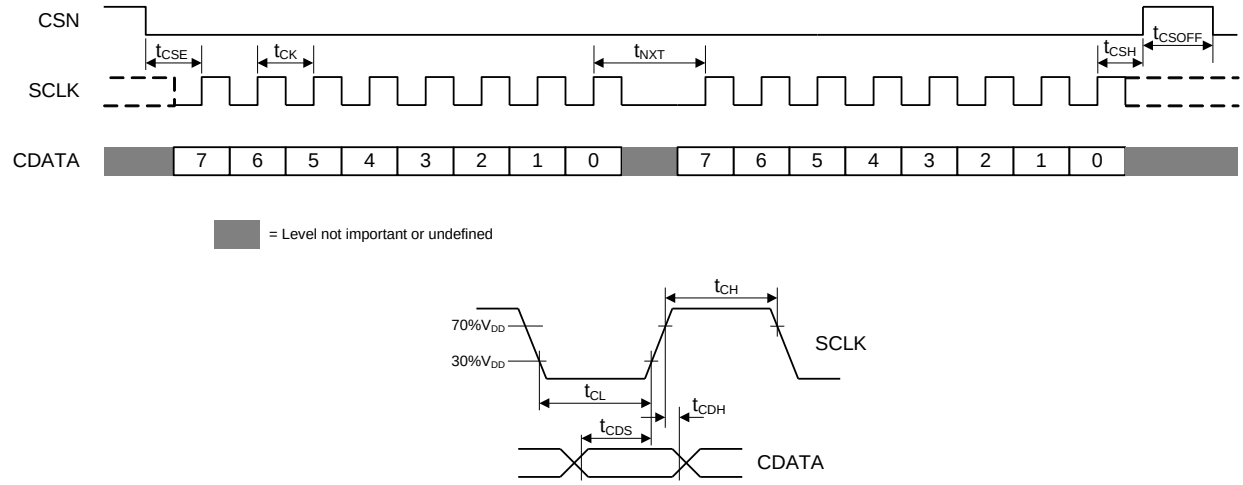
Notes:

4. Local oscillator input frequency twice or four times the required operating frequency.
5. Output power reduced dB for dB with forward path attenuation.
6. Peak power: PEP measured with 2-tone signal (two equal amplitude tones).
7. Measured between noise floor and mean power in a two-tone modulated wanted signal.
8. Measured at 400MHz, 5MHz offset over specified Forward Path Output Power range and with forward path attenuation between 0dB and –5dB. NB: typical noise performance achieved at typical output power and above.
9. Measured at 400MHz, 5MHz offset with specified Forward Path Output Power for relevant attenuation level.

10. Typical output power is achieved with the typical input drive level stated on I and Q channels, operation at 500MHz (sine and cosine waveforms on I and Q respectively).
11. Two tone test, limit met at all gain steps for 'Forward Path Output Power Level (PEP)' of: maximum output power below 600MHz, typical output power 600-900MHz, and 0dBm above 900MHz.
12. Measured with modulated output signal at relevant output power for forward path attenuations as specified.
13. Operating into a virtual earth (not ground).
14. Normally connected to BVREF pin via RC filter, the tolerance of BV_{REF} is specified in the DC Parameter table and these same tolerance limits apply here.
15. With a load of 1kΩ in parallel with 100pF. (Note 17 also applies).
16. Includes all IMD products up to and including the 7th order products e.g. 2nd, 3rd, 5th etc. Specification limit applies to each IMD product, not composite power of all products.
17. For small signal operation. It is recommended that for this application the input levels be restricted to +/-0.4V about a defined reference voltage of 1.6V (nominal); this will allow for some tolerance in components and for the precision of the reference voltage setting.
18. The inputs are protected with diodes. These diodes prevent the inadvertent application of voltages that may cause damage to the input transistors.
19. Two-tone test with value measured relative to power in either tone, unity gain, 0.8V p-p signal with two tones at 70kHz and 90kHz (400mV p-p each tone).
20. The output power appropriate for a particular application depends on the type of modulation and the spectral purity requirements in each particular case. For some applications it may be necessary to operate the output level below the specified typical level in order to achieve the desired results. Note also that the intermodulation performance, which influences the achievable output level, varies with frequency, see Note 11.
21. This is the impedance that should be presented to the output of the up-converter, e.g. using a balun. The precise load impedance may be optimised for a given operating frequency, or band of frequencies, to achieve improved output level and signal-to-noise ratio.
22. With a spurious-free LO input and specified output level.
23. Measured with MODIN, MODIP, MODQN, MODQP connected to BV_{REF} with 10Ω resistors decoupled by 33nF capacitors.
24. Voltage gain measured from modulator input (MODIN or MODQN) to output of a 4:1 balun, using 7kHz sine/cosine waves on MODIN/MODQN.
25. Measured at 20MHz offset from the operating frequency, all modulator I/Q inputs at BV_{REF}.
26. Performance measured based on IS-95B section 6.1.4.1.1; measurement bandwidths 1.23MHz for wanted and 3rd adjacent channel and 30kHz for 1st and 2nd adjacent channels.
27. LO divide by 2 mode operation only.
28. LO divide by 4 mode is not recommended for output frequencies below 50MHz.
29. Specification applies over the range 100MHz to 1GHz.
30. A typical figure at 40MHz or 50 MHz is –146dBc/Hz at a 5MHz offset.
31. The maximum value is derived from analysis of statistical evaluation results and is not guaranteed by 100% testing.
32. Gain and Output Power will reduce below 100MHz. Values are typically 4dB lower at 30MHz.
33. For operation with a modulator output above 600MHz optimum performance will typically be achieved with the LO input level in the range -15dBm to -20dBm.

C-BUS Timings (See Figure 9)		Notes	Min.	Typ.	Max.	Units
t_{CSE}	CSN-Enable to Clock-High Time		100	-	-	ns
t_{CSH}	Last Clock-High to CSN-High Time		100	-	-	ns
t_{CSOFF}	CSN-High Time between transactions		1.0	-	-	µs
t_{NXT}	Inter-Byte Time		200	-	-	ns
t_{CK}	Clock-Cycle Time		200	-	-	ns
t_{CH}	Serial Clock (SCLK) - High Time		100	-	-	ns
t_{CL}	Serial Clock (SCLK) - Low Time		100	-	-	ns
t_{CDS}	Command Data (CDATA) - Set-Up Time		75.0	-	-	ns
t_{CDH}	Command Data (CDATA) – Hold Time		25.0	-	-	ns

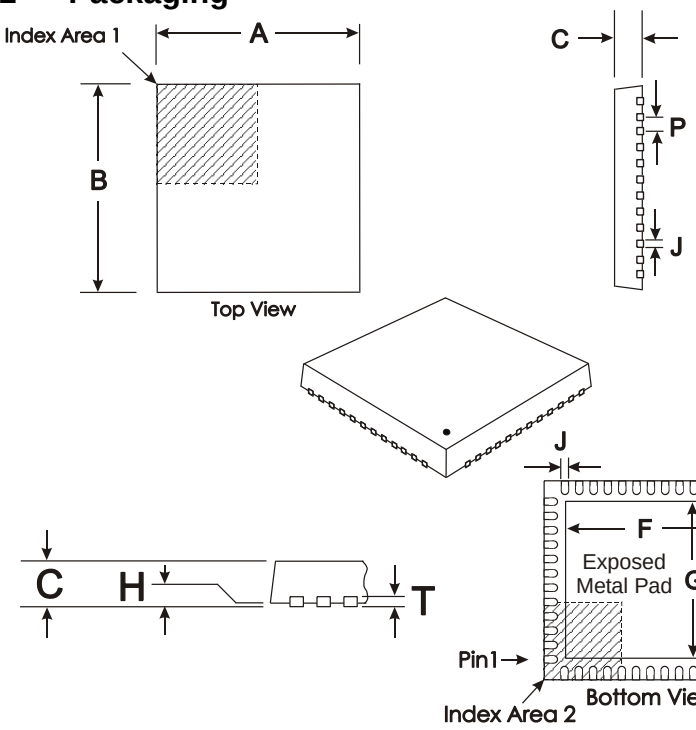
Maximum 30pF load on each C-BUS interface line.



Note: *Only 1 byte of data is used in CMX993/CMX993W C-BUS transactions.*

Figure 9 C-BUS Timing

8.2 Packaging

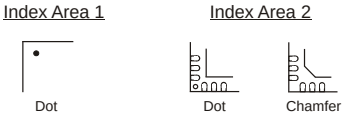


DIM.	MIN.	TYP.	MAX.
* A		7.00 BSC	
* B		7.00 BSC	
C	0.80	0.90	1.00
F	4.60		5.65
G	4.60		5.65
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees



Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Note:

In this device, the underside of the Q3 package must be electrically connected to the analogue ground. The circuit board should be designed so that no unwanted short circuits can occur.

Figure 10 Q3 Mechanical Outline: *Order as part no.* CMX993*Q3 or CMX993WQ3*

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