

# CMX017 UHF FM/FSK Transmitter

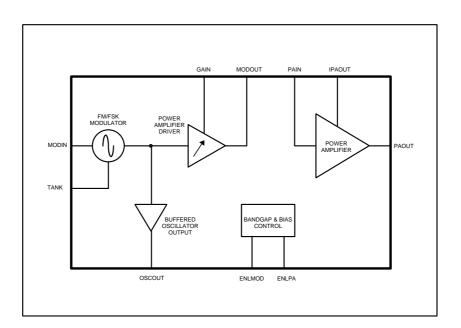
D/017/3 April 1999 Advance Information

#### **Features**

- Direct FM/FSK UHF Modulator
- Adjustable Modulator Output Power
- Integrated Power Amplifier with Output Power up to +20dBm (100mW)
- Low Power 2.7V Operation
- Powersave and Zero-Power (<10μA) Modes</li>
- 28-Pin SSOP Package

## **Applications**

- General Radio Link 860-965 MHz
- General 915MHz ISM Band (USA)
- Spread Spectrum Wireless Systems
- Fixed Frequency Transmissions
- Analogue/Digital Cordless Phones
- Handheld Data Terminals
- So-Ho Wireless Data Links



## 1.1 Brief Description

The CMX017 is a single chip UHF FM/FSK transmitter that combines both the RF VCO Modulator and RF Power Amplifier. It is suitable for both audio FM and digital FSK transmissions.

A buffered oscillator output provides the RF signal drive to an external synthesizer or fixed frequency phase-locked loop for channel frequency selection. Modulator output power is adjustable over a 20dB range and the integrated power amplifier delivers up to +20dBm. The device also includes a powersave mode: "Transmit Standby" and a zero-power mode: "Sleep". These allow independent power down control of both the modulator and power amplifier, thereby maximising battery life. The device can be used in conjunction with the CMX018, a double-conversion super-heterodyne receiver, to implement a complete UHF radio link.

## **CONTENTS**

<u>Section</u>	age
1.0 Features and Applications	.1
1.1 Brief Description	.1
1.2 Block Diagram	. 3
1.3 Signal List	. 4
1.4 External Components	. 6
1.5 General Description	
1.5.1 FM/FSK Modulator + PA Driver	. 7
1.5.2 Power Amplifier	
1.5.3 Powersave and Zero-Power Modes	.7
1.6 Application Notes	. 8
1.6.1 Generation of the Modulated RF Signal	. 8
1.6.2 Powersave and Zero-Power Modes	. 9
1.6.3 Lower Power Applications	. 9
1.6.4 Example Schematic and Layout	. 9
1.7 Performance Specification	12
1.7.1 Electrical Performance	
1.7.2 Packaging	
1.7.3 Handling Precautions	14

**Note:** As this product is still in development, it is likely that a number of changes and additions will be made to this specification. Items marked TBD or left blank will be included in later issues. Information in this data sheet should not be relied upon for final product design.

## 1.2 Block Diagram

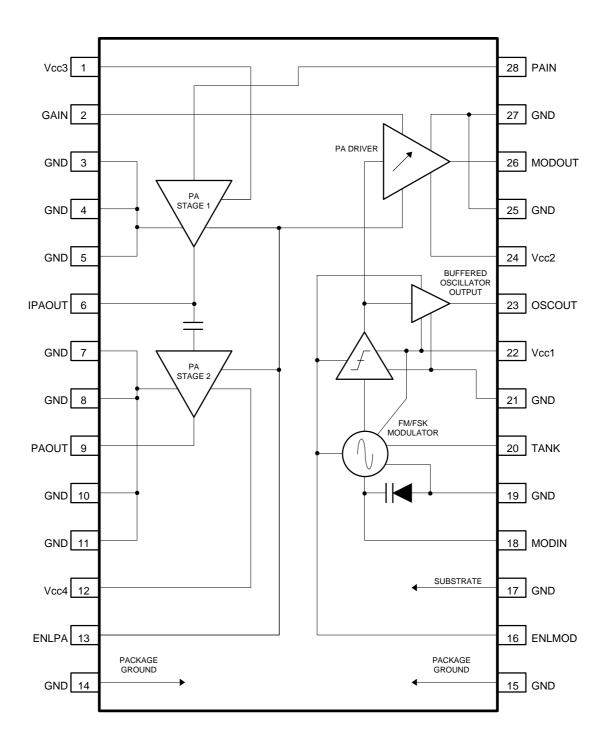


Figure 1 Internal Block Diagram

## 1.3 Signal List

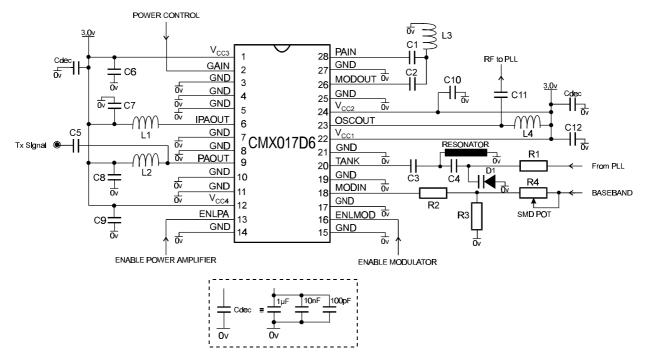
Package D6	Signal		Description		
Din No	Nama	T			
Pin No.	Name	Туре			
1	Vcc3	POWER	Power amplifier (first stage) power supply - nominally 3.0V		
2	GAIN	I/P	Modulator output (pin 26) - Power Control		
3	GND	GROUND	Ground-plane connection to the power amplifier		
4	GND	GROUND	Ground-plane connection to the power amplifier		
5	GND	GROUND	Ground-plane connection to the power amplifier		
6	IPAOUT	O/P	Output (open-collector) from the first stage of the power amplifier		
7	GND	GROUND	Ground-plane connection to the power amplifier		
8	GND	GROUND	Ground-plane connection to the power amplifier		
9	PAOUT	O/P	Output (open-collector) from the second stage of the power amplifier		
10	GND	GROUND	Ground-plane connection to the power amplifier		
11	GND	GROUND	Ground-plane connection to the power amplifier		
12	Vcc4	POWER	Power amplifier (second stage) power supply - nominally 3.0V		
13	ENLPA	CMOS I/P	Power Amplifier powersave logic control. A logic '0' powers down the Power Amplifier and Driver stages		
14	GND	GROUND	Ground-plane connection		
15	GND	GROUND	Ground-plane connection		
16	ENLMOD	CMOS I/P	Modulator zero-power logic control. A logic '0' powers down the Modulator and Buffered Oscillator stages		
17	GND	GROUND	Ground-plane connection		
18	MODIN	I/P	Baseband modulation input signal		
19	GND	GROUND	Ground-plane connection to the VCO		
20	TANK	I/P	VCO Tank circuit/Resonator connection		

Package D6	Signal Description		
Pin No.	Name	Туре	
21	GND	GROUND	Ground-plane connection to the modulator and VCO buffer
22	Vcc1	POWER	Modulator power supply - nominally 3.0V
23	OSCOUT	O/P	Buffered Oscillator (open-collector) output
24	Vcc2	POWER	Power Amplifier Driver power supply - nominally 3.0V
25	GND	GROUND	Ground-plane connection for the Power Amplifier Driver
26	MODOUT	O/P	Modulator output
27	GND	GROUND	Ground-plane connection for the Power Amplifier Driver
28	PAIN	I/P	Power Amplifier input

Input Output Notes: I/P

O/P

## 1.4 External Components



## **Component Values:**

L1	1.5nH	
L2	22nH	
L3	6.8nH	
L4	22nH	
D1	Varactor	Varactor Diode, type SMV1233-011
~	Resonator	Co-Axial Resonator, type RG402, length = 11mm, shorted end.
C1	5.6pF	
C2	33pF	
C3	4.3pF	
C4	6.8pF	
C5	100pF	
C6	100pF	
C7	100pF	
C8	100pF	
C9	100pF	
C10	100pF	
C11	100pF	
C12	100pF	
R1	10kΩ	
R2	10k $\Omega$	
R3	<b>TBD</b> kΩ	(value is application dependent)
R4	<b>TBD</b> $k\Omega$	SMD Potentiometer (value is application dependent)

NOTE: Components are surface mount, type SMD0603, unless otherwise marked.

Figure 2 Example of CMX017 with External Components

## 1.5 General Description

The CMX017 is a single chip UHF FM/FSK transmitter that combines both the RF VCO Modulator and RF Power Amplifier. It is suitable for both audio FM and digital FSK transmissions.

A buffered oscillator output provides the RF signal drive to an external synthesizer or fixed frequency phase-locked loop for channel frequency selection. Modulator output power is adjustable over a 20dB range and the integrated power amplifier delivers up to +20dBm. The device also includes a powersave mode: "Transmit Standby" and a zero-power mode: "Sleep". These allow independent power down control of both the modulator and power amplifier, thereby maximising battery life. The device can be used in conjunction with the CMX018, a double-conversion super-heterodyne receiver, to implement a complete UHF radio link.

#### 1.5.1 FM/FSK Modulator + PA Driver

The modulator circuit uses an integrated oscillator whose frequency can be directly modulated by the DC-coupled input base-band signal, at the MODIN pin, to generate a frequency modulated (FM or FSK) RF signal. The oscillator requires an external varactor and resonator circuit, connected at the TANK pin, to tune to the required RF channel. A buffered oscillator signal is provided from an open-collector output, at the OSCOUT pin, to drive an external frequency synthesizer for the channel selection.

The output power, at the MODOUT pin, is variable over a 20dB range. The output power is maximum when the GAIN pin is connected to Vcc and is reduced by typically 20dB when this pin is connected to 0V. The output impedance at the MODOUT pin is typically  $50\Omega$ .

## 1.5.2 Power Amplifier (PA)

The power amplifier has two internal stages, each biased for class-B operation, and is designed to have a fixed overall power gain. The input and output impedances can be terminated with  $50\Omega$ . A typical power gain improvement of 2dB is achieved using simple external matching networks.

## 1.5.3 Powersave and Zero-Power Modes

The Modulator and Buffered Oscillator stages are powered down independently of the PA Driver and Power Amplifier stages, by means of the ENLMOD and ENLPA logic inputs:

A logic '0' at ENLMOD powers down the Modulator and Buffered Oscillator stages. A logic '0' at ENLPA powers down the PA Driver and Power Amplifier stages.

Refer to the block diagram in Figure 1 and to the Applications Section 1.6.2.

## 1.6 Application Notes

## 1.6.1 Generation of the Modulated RF Signal

The modulator on the CMX017 relies on the direct modulation of the RF Voltage Controlled Oscillator (VCO), which is stabilised to the channel centre frequency by an external Frequency Synthesizer or Phase Locked Loop (PLL). The user has control over the external PLL filter and VCO tank components and choice of these components will have an impact upon the following PLL parameters:

Closed loop bandwidth, settling time and transient response Modulation linearity VCO phase noise

Three modulation requirements may be achieved as follows:

#### a) The minimum modulation signal frequency is above the PLL Closed Loop Bandwidth

In applications where the transmit channel frequency is fixed or occasionally changed, a narrow PLL bandwidth can be chosen such that the minimum modulation frequency is in excess of the PLL bandwidth. With the PLL active whilst the base-band signal is applied to the modulator there will be negligible distortion of the modulated RF output signal. A benefit of this technique is that an output phase noise improvement is achieved, compared to the free running VCO phase noise characteristic.

## b) The minimum modulation signal frequency is within the PLL Closed Loop Bandwidth

In Frequency Hopped Spread Spectrum applications the frequency synthesizer must be agile. Consequently the PLL bandwidth should be designed to achieve the required hop rate and, in most systems, this bandwidth will exceed the minimum modulation frequency. With the PLL active during modulation, the loop will compensate for the signal frequency components within the loop bandwidth, introducing a frequency dependant distortion of the modulated RF output signal.

To avoid the modulation distortion the carrier frequency is tuned by the external synthesizer chip, with no modulating signal applied. The synthesizer control is then disabled, by setting the charge-pump output of the synthesizer to tri-state. The DC coupled baseband signal, applied to the MODIN pin, then modulates the free running VCO to generate the FM or FSK output signal.

# c) A flat modulator response is required down to DC, whilst benefiting from the phase noise improvements due to the PLL (Two-Point Modulation)

Unlike in the above two cases, where a fixed reference frequency is used in the PLL, the Two-Point Modulation technique requires modulation inputs to both the PLL reference oscillator and to the RF VCO circuits.

The modulation signal should be applied to both modulation inputs with suitable AC/DC levels and with the correct phase to achieve cancellation of the loop's feedback. This prevents the radio's PLL circuitry from counteracting the modulation process and so provides a clean flat modulation response down to DC.

#### 1.6.2 Powersave and Zero-Power Modes

It is possible to power down each section of the transmitter independently. This feature may be useful when the CMX017 is configured, with the CMX018, as a radio transceiver. It allows the transmitter to be powered on and off, thereby saving power, during the sleep and standby periods.

In **SLEEP** mode (ENLMOD = '0' and ENLPA = '0') all sections of the device are powered down and the current consumption is reduced to less than  $10\mu$ A. This is the zero-power mode.

In **TRANSMIT-STANDBY** mode (ENLMOD = '1' and ENLPA = '0') only the PA Driver and Power Amplifier stages are powered down, whilst the Modulator and Buffered Oscillator remain active. This powersave mode allows the external frequency synthesizer to stabilise the channel centre -frequency prior to the RF transmission.

In **TRANSMIT** mode (ENLMOD = '1' and ENLPA = '1') both the Modulator and Power Amplifier sections of the device are fully operational.

**Note:** The device can be used as a stand alone "**UHF Power Amplifier**" by forcing (ENLMOD = '0' and ENLPA = '1'). The efficiency is maximised by connecting the Vcc2 pin to 0V. (The Vcc1 pin must remain connected to 3.0V.)

#### 1.6.3 Lower Output Power Applications

For very short range applications the antenna drive can be taken from the modulator output, MODOUT, at pin 26. The Power Amplifier is powered down by connecting Vcc3 and Vcc4 (pins 1 and 12) to 0V. This allows the supply current to be minimised and the Modulator output to be enabled or disabled using the ENLPA input at pin 13.

## 1.6.4 Example Schematic and Layout

The following schematic (Figure 3) and printed circuit layout (Figure 4) show a typical application interface for the CMX017. To aid legibility, the schematic and layout are available electronically from the CML website <a href="http://www.cmlmicro.co.uk">http://www.cmlmicro.co.uk</a> or on floppy disk by request from CML's office. Alternative components and component values are shown on the schematic. These should be selected according to the intended application. The schematic uses the following ICs:

U2 IC Works WB1315X U4 Analog Devices AD8532-SO8

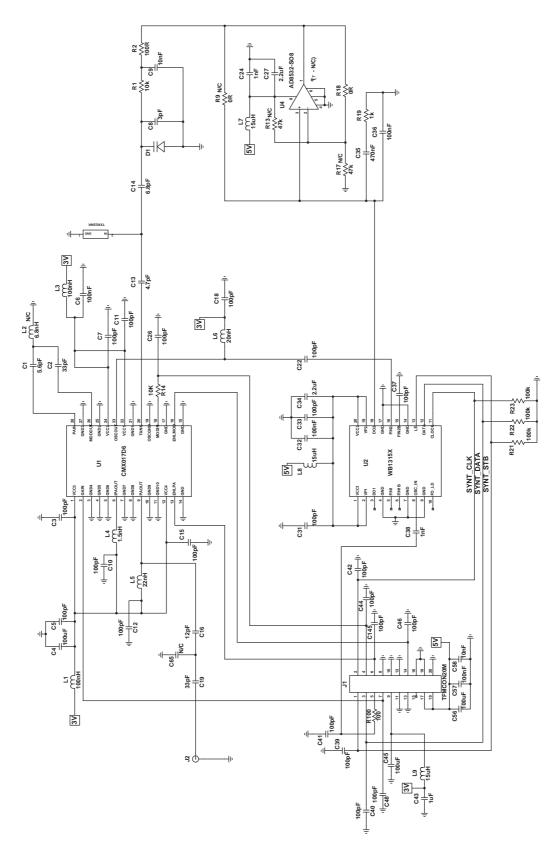


Figure 3 Application Schematic

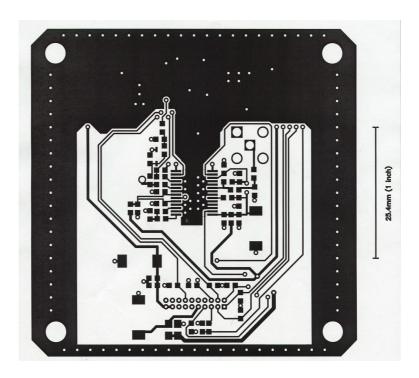


Figure 4a Application Layout - Top Copper

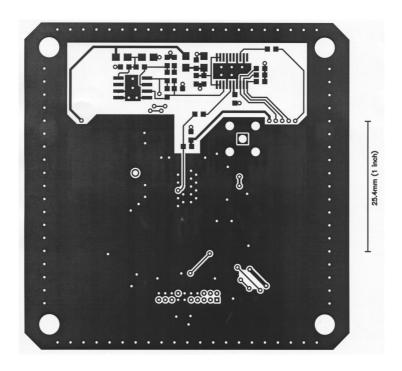


Figure 4b Application Layout - Bottom Copper (not reversed)

Available from http://www.cmlmicro.co.uk

## 1.7 Performance Specification

## 1.7.1 Electrical Performance

## **Absolute Maximum Ratings**

Exceeding these maximum ratings can result in damage to the device.

	Pin	Min.	Max.	Units	
Supply (Vcc)	1, 12, 22, 24	-0.3	7.0	V	
Input Voltage	2, 13, 16, 18, 20	-0.3	Vcc + 0.3	V	
Power Amplifier Input Power	28		+7	dBm	

D6 Package	Min.	Max.	Units	
Total Allowable Power Dissipation at Tamb = 25°C		1100	mW	
Derating		11	mW/°C	
Storage Temperature	-55	+125	°C	

## **Operating Limits**

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (Vcc)		2.7	3.3	V
Operating Frequency Range		860	965	MHz
Operating Temperature		-10	+60	°C

## **Operating Characteristics**

For the following conditions unless otherwise specified:

Vcc = 2.7V to 3.3V, Tamb = -10°C to +60°C, RF = 915MHz,  $50\Omega$  source and load impedance.

	Pin	Min.	Тур.	Max.	Units
DC Parameters					
Device Fully Enabled (ENLPA=HI and ENLMOD=HI)					
Icc <sup>1</sup> [Output Power = +20dBm at PAOUT (Pin 9)]		-	130	-	mA
Icc <sup>1</sup> [Output Power = +10dBm at PAOUT (Pin 9)]		-	60	-	mA
Icc <sup>1</sup> [Output Power = 0dBm at PAOUT (Pin 9)]		-	40	-	mA
Device in Power-Down Modes					
Icc <sup>1</sup> in <b>STANDBY</b> mode (ENLPA = LO and ENLMOD = HI)		-	24	-	mA
Icc <sup>1</sup> in <b>SLEEP</b> mode (ENLPA = LO and ENLMOD = LO)		-	TBD	10	μΑ
AC Parameters					
Modulator, VCO Buffer and PA Driver					
Output Power [GAIN (pin 2) at Vcc]	26	-	-4.0	-	dBm
Output Power [GAIN (pin 2) at 1.5V]	26	-	-9.0	-	dBm
Output Power [GAIN (pin 2) at 1.0V]	26	-	-14	-	dBm
Buffered VCO Output at OSCOUT pin <sup>2</sup>	19	-	-10	-	dBm
Oscillator Second Harmonic Output <sup>3</sup>	26	-	-25	-	dBc
Oscillator Third Harmonic Output <sup>3</sup>	26	-	-35	-	dBc
Modulation Sensitivity <sup>4</sup>	18	-	0.4	-	MHz/V
Maximum Deviation <sup>5</sup>	26	-	1.5	-	MHz
Input Data Rate	18	-	-	TBD	kBits/S
Output VSWR (at maximum output power)	26	-	TBD	-	
Power Amplifier					
Power Gain	28, 9	-	22	-	dB
Power Gain (with external matching at Vcc = 3.3V)	28, 9	-	24	-	dB
Maximum Power Gain Variation (	28, 9	-	2.0	-	dB
Maximum Power Gain Variation <sup>6</sup> (with matching)	28,9	-	1.5	-	dB
Input 1dB Compression Point	9	-	+1.0	-	dBm
Input 1dB Compression Point (with matching)	9	-	0	-	dBm
Reverse Isolation	9, 28	-	-35	-	dB
Output VSWR (at maximum output power)	9	-	TBD	-	

## Notes:

- 1. Total current from the external 3.0V power supply.
- 2. Power measured into a  $50\Omega$  load.
- 3. With external matching.
- 4. Stepped modulation voltage input from 1.0V to 2.0V.
- 5. Stepped modulation voltage from 0V to 3.0V.
- 6. Input Power = -15dBm to -1dBm.

UHF FM/FSK Transmitter CMX017

## 1.7.2 Packaging

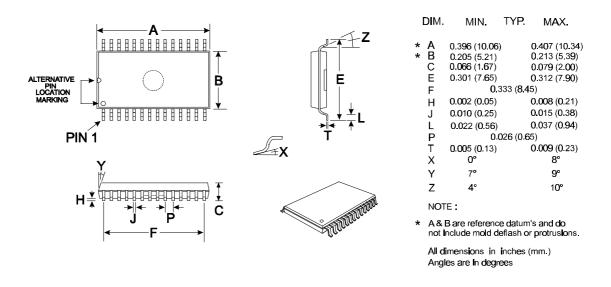


Figure 5 28-Pin Plastic SSOP Mechanical Outline: Order as part no. CMX017D6

## 1.7.3 Handling Precautions

This device is a high performance RF integrated circuit and is ESD sensitive. Adequate precautions must be taken during handling and assembly of this device.

CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.



1 WHEATON ROAD WITHAM - ESSEX CM8 3TD - ENGLAND Telephone: +44 1376 513833
Telefax: +44 1376 518247
e-mail: sales@cmlmicro.co.uk
http://www.cmlmicro.co.uk