CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX7131/CMX7141 Analogue PMR I/Q Processor

D/7131/7141_FI8.x/6 September 2013

DATASHEET

Advance Information

7131/7141FI-8.0.x: Analogue PMR Baseband Processor with I/Q Downconversion Interface, Auxiliary System Clocks, ADCs and DACs

Features

- Analogue PMR
  - Voice Processing (EN 300 086 / EN 300 296 / TIA-603 compliant)
  - Voice Compander
  - Selectable Filters for 12.5kHz/25kHz Operation
  - 1200 bps FFSK Modem (MPT1327 compatible)
  - Selcall Encoder/Decoder (16 tones)
  - DTMF Encoder/Decoder (16 tones)
  - CTCSS / DCS Encoder/Decoder
  - CTCSS tone phase reversal facility in Tx and Rx
  - Audio Tone Generator
  - Frequency Inversion Voice Scrambler
  - Squelch Function
  - RSSI Measurement

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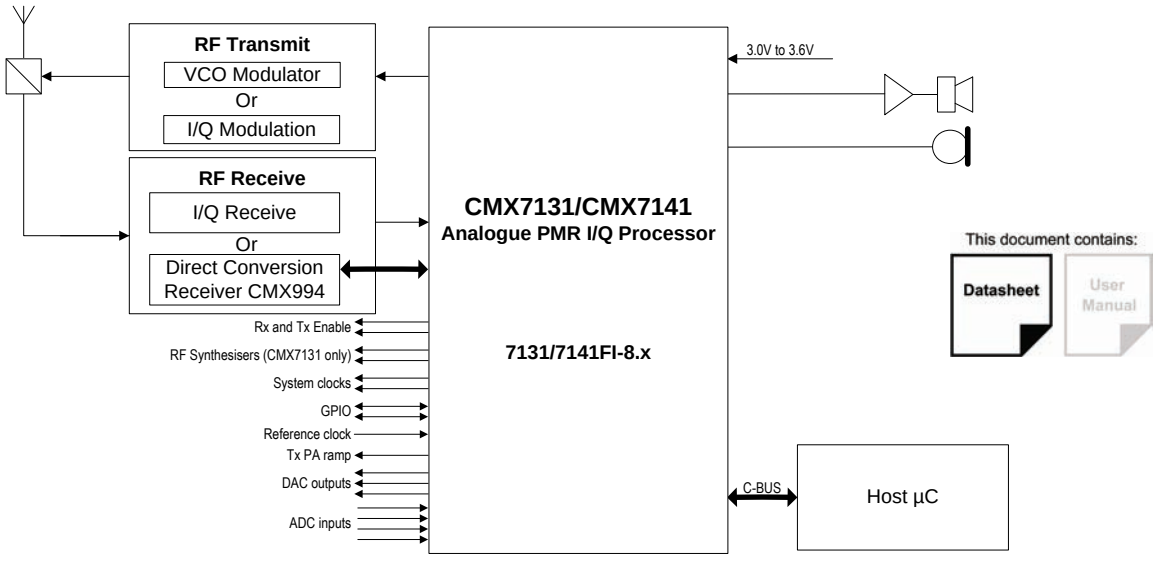
Additional Features

- 2 Auxiliary ADCs (4 Multiplexed Inputs)
- 4 Auxiliary DACs
- 2 Auxiliary System Clock Outputs
- Tx Outputs for Two-point or I/Q Modulation
- Rx Inputs for CMX994 Direct Conversion (I/Q) Receiver
- C-BUS Serial Interface to CMX994 Transceiver
- Automatic DC Offset Removal
- AGC Management
- Signal to Noise Optimisation
- 2 RF Synthesisers (CMX7131 only)
- C-BUS Serial Interface to Host Micro
- Flexible Powersave Modes
- Low-power (3.3V) Operation
- Available in LQFP or VQFN Packages



1 Brief Description

The device utilises CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™; this is a data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from the host microcontroller over the C-BUS serial interface. The device's functions and features may be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades. This document refers specifically to the features provided by Function Image™ 7131/7141FI-8.0.x.x.

The 7131/7141FI-8.0.x Function Image™ (FI) implements half-duplex Analogue PMR signal processing, including voice processing, 1200bps FFSK modem, CTCSS/DCS (with CTCSS tone phase reversal facility), DTMF and Selcall signalling. In conjunction with a suitable host and a Direct Conversion (I/Q) Receiver (CMX994), a compact, low-cost, low-power analogue PMR radio conforming to ETSI standards EN 300 086 / EN 300 296 and TIA-603 can be realised. Operation is tailored for the CMX994 Direct Conversion Receiver IC with automatic control of dc offset, AGC, etc. Dual mode, analogue/digital PMR operation can also be achieved with the CMX7131/CMX7141 by re-loading the device with any of the 7131/7141 family of FI's that supports a I/Q interface in receive mode.

The embedded functionality of the CMX7131/CMX7141 manages the CMX994 downconverter autonomously (via the Auxiliary SPI/C-BUS interface) thus minimises host microcontroller interactions enabling the lowest operating power and therefore the longest battery life for a PMR radio. The CMX7131/CMX7141 automatic powersave mode gives the ability to significantly reduce the average power consumption of the overall solution.

Other features include two auxiliary ADCs with four selectable inputs and four auxiliary DAC interfaces (with an optional RAMDAC on the first DAC output, to facilitate transmitter power ramping). Additionally the CMX7131 features two on-chip RF synthesisers, with easy Rx/Tx frequency changeover.

The CMX7141 is identical in functionality to the CMX7131 with the exception that the two on-chip RF synthesisers have been deleted, which enables it to be supplied in a smaller package. This document refers to both parts, unless otherwise stated. Each device is available in both LQFP and VQFN packages.

Note that text shown in pale grey indicates features that will be supported in future versions of the Function Image™.

This datasheet is the first part of a two-part document comprising datasheet and user manual: the user manual can be obtained by registering your interest in this product with your local CML representative.

CONTENTS

Table Page

Figure Page

History

Version	Changes	Date
6	• Correct FM Hum and noise specifications • TX I/Q Functionality greyed-out • Figure 12, Figure 13 and Figure 14 improved clarity • Function image updates section added	September 2013
5	• Add DTMF signalling • Add CTCSS tone phase reversal • Update 994 pass-through mode documentation	July 2013
4	• Figure 12, 13 and 14 replaced to show improved detail on X and Y axes. • Figure 29 - correct diagram now included for Q3 package. • CMX994 Pass-through Mode documentation added	June 2013
3	• Additional information on powersave, RSSI measurement, frequency measurement and performance of the CMX7131/41 + CMX994 combination. • Current consumption data added • Figure 6 corrected • Editorial corrections and clarifications • Updated RAMDAC and tone generator descriptions in section 8.1.4 • Expanded description of Fine Level adjustment of outputs in section 8.1.24	May 2013
2	• Remove references to EEPROM/Serial Flash boot mode • Improve adjacent/alternate channel rejection using AuxADC1 • Add Parametric figures following evaluation	Jan 2013
1	• Original document	Nov 2012

This is Advance Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document.
Information in this datasheet should not be relied upon for final product design.

2 Block Diagram

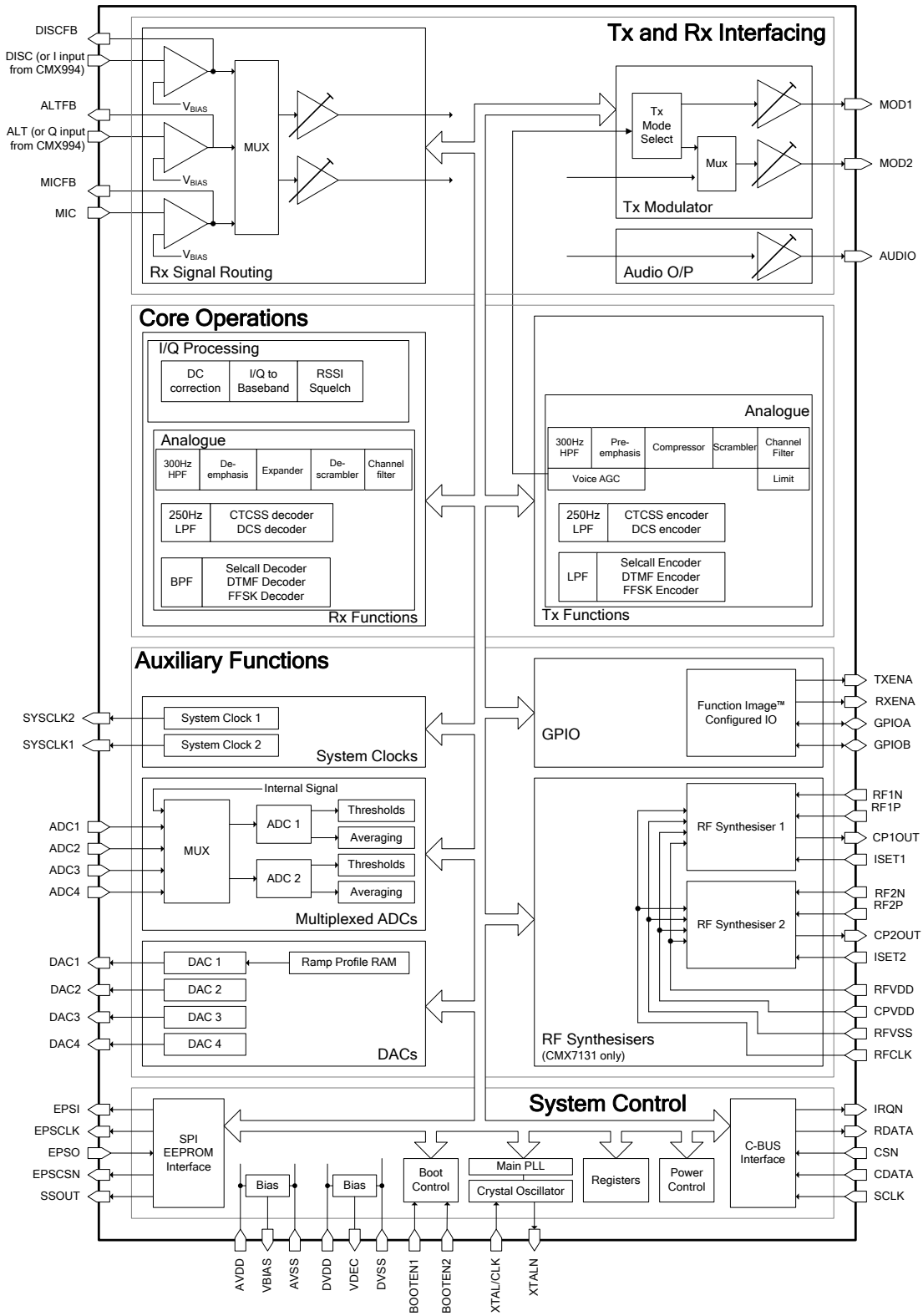


Figure 1 Block Diagram

3 Pin and Signal List

CMX7131 64-pin Q1/L9	CMX7141 48-pin Q3/L4	Pin Name	Type	Description
1	**8**	IRQN	OP	C-BUS: A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor (R1) is required.
2	-	RF1N	IP	RF Synthesiser 1 Negative Input
3	-	RF1P	IP	RF Synthesiser 1 Positive Input
4	-	RFVSS	PWR	Negative supply rail (ground) for RF Synthesiser 1
5	-	CP1OUT	OP	RF Synthesiser 1 Charge Pump output
6	-	ISET1	IP	RF Synthesiser 1 Charge Pump Current Set input
7	-	RFVDD	PWR	The 2.5V positive supply rail for both RF Synthesisers. This should be decoupled to RFV_{SS} by a capacitor mounted close to the device pins.
8	-	RF2N	IP	RF Synthesiser 2 Negative Input
9	-	RF2P	IP	RF Synthesiser 2 Positive Input
10	-	RFVSS	PWR	The negative supply rail (ground) for RF Synthesiser 2
11	-	CP2OUT	OP	RF Synthesiser 2 Charge Pump output
12	-	ISET2	IP	RF Synthesiser 2 Charge Pump Current Set input
13	-	CPVDD	PWR	The 3.3V positive supply rail for the RF Synthesiser charge pumps. This should be decoupled to RFV_{SS} by a capacitor mounted close to the device pins.
14	-	RFCLK	IP	RF Clock Input (common to both RF Synthesisers)[1]
15	**11**	GPIOA	OP	General Purpose I/O pin
16	**12**	GPIOB	OP	General Purpose I/O pin
17	-	-	NC	*Reserved* – do not connect this pin
18	**9**	VDEC	PWR	Internally-generated 2.5V digital supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for optional connection to RFV_{DD}.
19	**10**	RXENA	OP	Rx Enable – active low when in Rx mode ($C1:b0 = 1)
20	**13**	SYSCLK1	OP	Synthesised Digital System Clock Output 1
21	**14**	DVSS	PWR	Digital ground
22	-	-	NC	*Reserved* – do not connect this pin
23	**15**	TXENA	OP	Tx Enable – active low when in Tx mode ($C1:b1 = 1)
24	**16**	DISC	IP	I input from CMX994
25	**17**	DISCFB	OP	I input amplifier feedback
26	**18**	ALT	IP	Q input from CMX994

[1] To minimise crosstalk, this signal should be connected to the same clock source as XTAL/CLK input.

CMX7131 64-pin Q1/L9	CMX7141 48-pin Q3/L4	Pin Name	Type	Description	
27	**19**	ALTFB	OP	Q input amplifier feedback	
28	**20**	MICFB	OP	Microphone input amplifier feedback	
29	**21**	MIC	IP	Microphone inverting input	
30	**22**	AVSS	PWR	Analogue ground	
31	**23**	MOD1	OP	Modulator output 1	
32	**24**	MOD2	OP	Modulator output 2	
33	**25**	VBIAS	OP	Internally-generated bias voltage of approximately $AV_{DD}/2$, except when the device is in 'Powersave' mode when V_{BIAS} will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed.	
34	**26**	AUDIO	OP	Audio Output	
35	**27**	ADC1	IP	Auxiliary ADC input 1	Each of the two ADC blocks can select its input signal from any one of these input pins, or from the MIC, ALT or DISC input pins. See Section 6.11 for details.
36	**28**	ADC2	IP	Auxiliary ADC input 2	
37	**29**	ADC3	IP	Auxiliary ADC input 3	
38	**30**	ADC4	IP	Auxiliary ADC input 4	
39	**31**	AVDD	PWR	Analogue +3.3V supply rail. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.	
40	**32**	DAC1	OP	Auxiliary DAC output 1/RAMDAC	
41	**33**	DAC2	OP	Auxiliary DAC output 2	
42	**34**	AVSS	PWR	Analogue ground	
43	**35**	DAC3	OP	Auxiliary DAC output 3	
44	**36**	DAC4	OP	Auxiliary DAC output 4	
-	**37**	DVSS	PWR	Digital Ground	
45	**38**	VDEC	PWR	Internally-generated 2.5V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for the optional connection to RFV_{DD}.	
46	**39**	XTAL/CLK	IP	Input from the external clock source or Xtal	
47	**40**	XTALN	OP	The output of the on-chip Xtal oscillator inverter. NC if external clock used.	
48	**41**	DVDD	PWR	Digital +3.3V supply rail. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins.	
49	**42**	CDATA	IP	C-BUS Command Data: Serial data input from the µC	
50	**43**	RDATA	TS OP	C-BUS Reply Data: A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.	
51	-	-	NC	*Reserved* – do not connect this pin	

CMX7131 64-pin Q1/L9	CMX7141 48-pin Q3/L4	Pin Name	Type	Description
53	**44**	SSOUT	OP	SPI bus Chip Select/Frame Sync
52	**45**	DVSS	PWR	Digital ground
54	**46**	SCLK	IP	C-BUS Serial Clock: The C-BUS serial clock input from the µC
55	**47**	SYSCLK2	OP	Synthesised Digital System Clock Output 2
56	**48**	CSN	IP	C-BUS Chip Select: The C-BUS chip select input from the µC - there is no internal pullup on this input
57	-	-	NC	*Reserved* – do not connect this pin
58	**1**	EPSI	OP	CMX994 Interface: Output; SPI bus Output
59	**2**	EPSCLK	OP	CMX994 Interface: Clock; SPI bus Clock
60	**3**	EPSO	IP+PD	CMX994 Interface: Input; SPI bus Input
61	**4**	EPSCSN	OP	CMX994 Interface: Chip Select
62	**5**	BOOTEN1	IP+PD	Used to determine the operation of the bootstrap program. Must be pulled high when operating CMX7141 with CMX994.
63	**6**	BOOTEN2	IP+PD	
64	**7**	DVSS	PWR	Digital ground
EXPOSED METAL PAD	EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad (which is exposed on Q1 and Q3 packages only) may be electrically unconnected or, alternatively, may be connected to analogue ground (AV_{SS}). **No other electrical connection is permitted.**

Notes: IP = Input (+ PU/PD = internal pullup **/** pulldown resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal.

3.1 Signal Definitions

Table 1 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
DV_{DD}	DVDD	Power supply for digital circuits
V_{DEC}	VDEC	Power supply for core logic, derived from DV_{DD} by on-chip regulator
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AV_{DD}
AV_{SS}	AVSS	Ground for all analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits
RFV_{DD}	RFVDD	Power supply for RF circuits
RFV_{SS}	RFVSS	Ground for RF circuits
CPV_{DD}	CPVDD	Power supply for charge pump circuits

4 Component and PCB Recommendations

4.1 Recommended External Components (Generic)

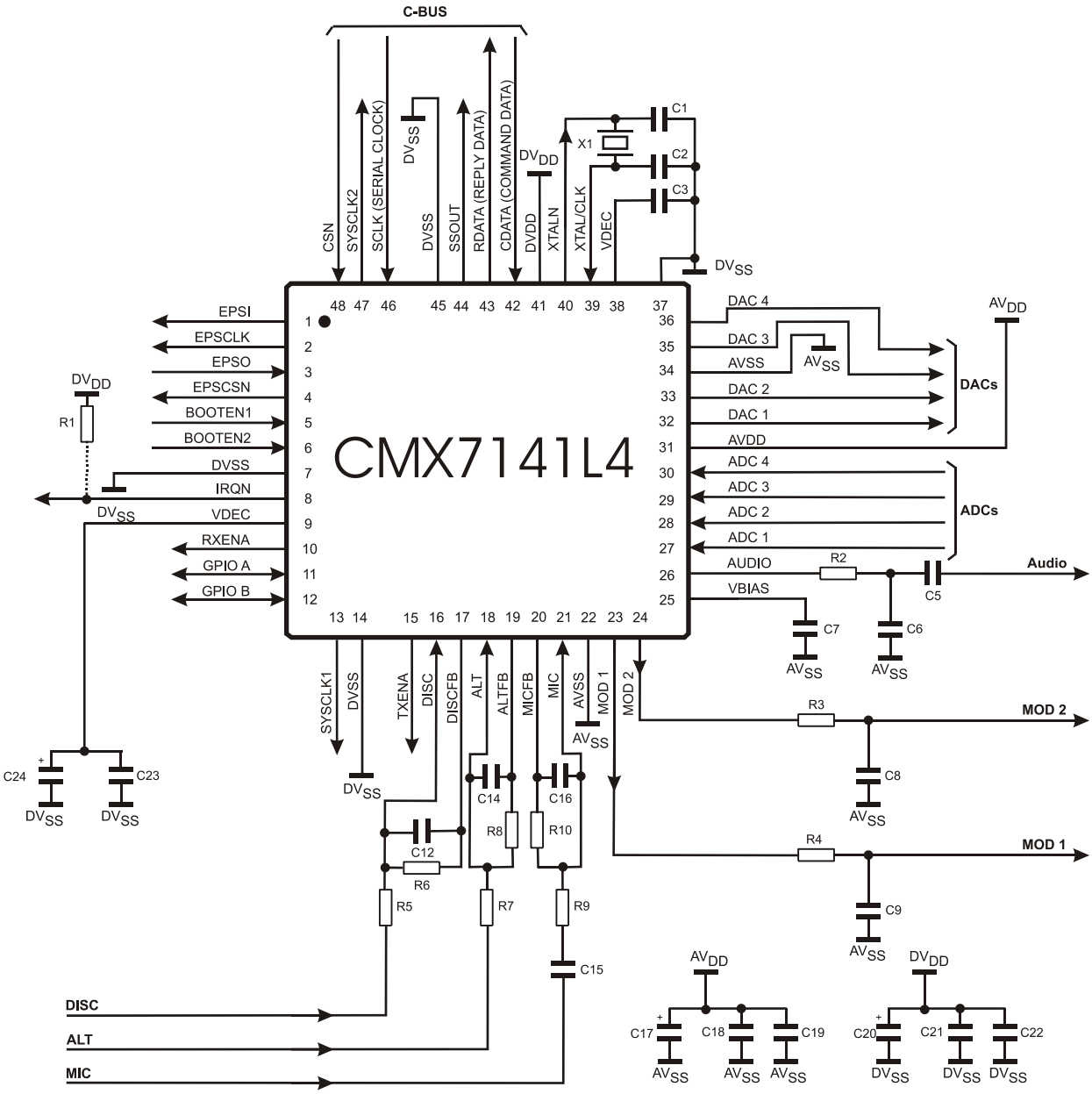


Figure 2 CMX7141 (L4 and Q3) Recommended External Components

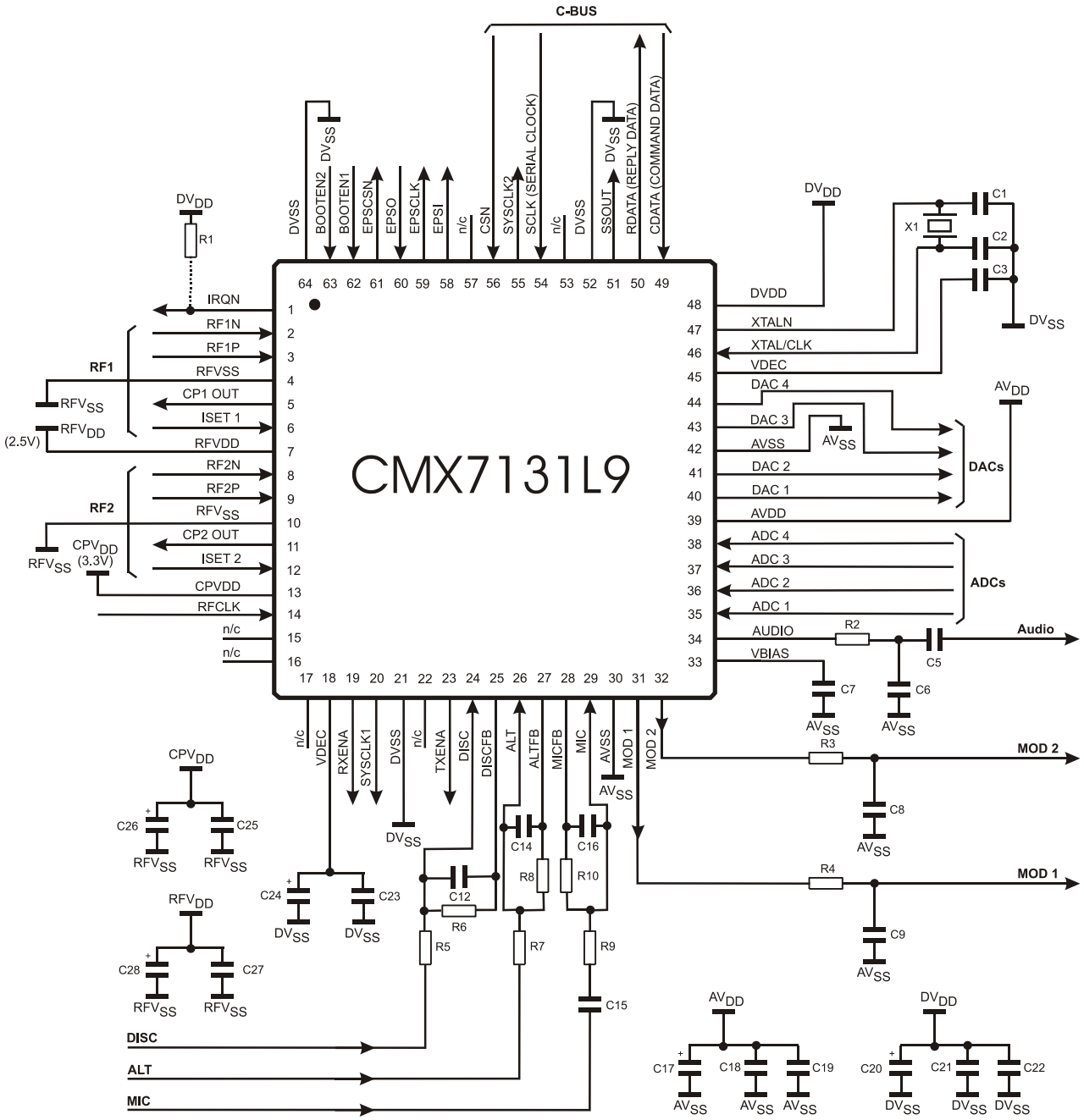


Figure 3 CMX7131 (L9 and Q1) Recommended External Components

Table 2 Recommended External Components

R1	100kΩ	C1	18pF	C11	*not used*	C21	10nF
R2	20kΩ	C2	18pF	C12	100pF	C22	10nF
R3	20kΩ	C3	10nF	C13	*not used*	C23	10nF
R4	20kΩ	C4	*not used*	C14	100pF	C24	10µF
R5	See note 2	C5	1nF	C15	See note 5		
R6	100kΩ	C6	100pF	C16	200pF		
R7	See note 3	C7	100nF	C17	10µF		
R8	100kΩ	C8	100pF	C18	10nF	X1	6.144MHz
R9	See note 4	C9	100pF	C19	10nF		See note 1
R10	100kΩ	C10	*not used*	C20	10µF		

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance. In 7131/7141FI-8.0.x.x, by default, a 19.2MHz oscillator is assumed (in which case X1, C1 and C2 are not required).

2. See section 4.3.

3. See section 4.3.

4. R9 should be selected to provide the desired dc gain (assuming C15 is not present) of the microphone input as follows:

$$|GAIN_{MIC}| = 100k\Omega / R9$$

   The gain should be such that the resultant output at the MICFB pin is within the microphone input signal range specified in 6.15.1. For optimum performance with low signal microphones, an additional external gain stage may be required.

5. C15 should be selected to maintain the lower frequency roll-off of the MIC input as follows:

$$C15 \geq 30nF \times |GAIN_{MIC}|$$

6. DISC/ALT and DISCFB/ALTFB connections allow the user to connect to an I/Q receiver (CMX994). These input paths should be dc coupled.

7. A single 10µF electrolytic capacitor (C24, fitted as shown) may be used for smoothing the power supply to both VDEC pins, providing they are connected together on the pcb with an adequate width power supply trace. Alternatively, separate smoothing capacitors should be connected to each VDEC pin. High frequency decoupling capacitors (C3 and C23) must always be fitted as close as possible to both VDEC pins.

4.2 PCB Layout Guidelines and Power Supply Decoupling

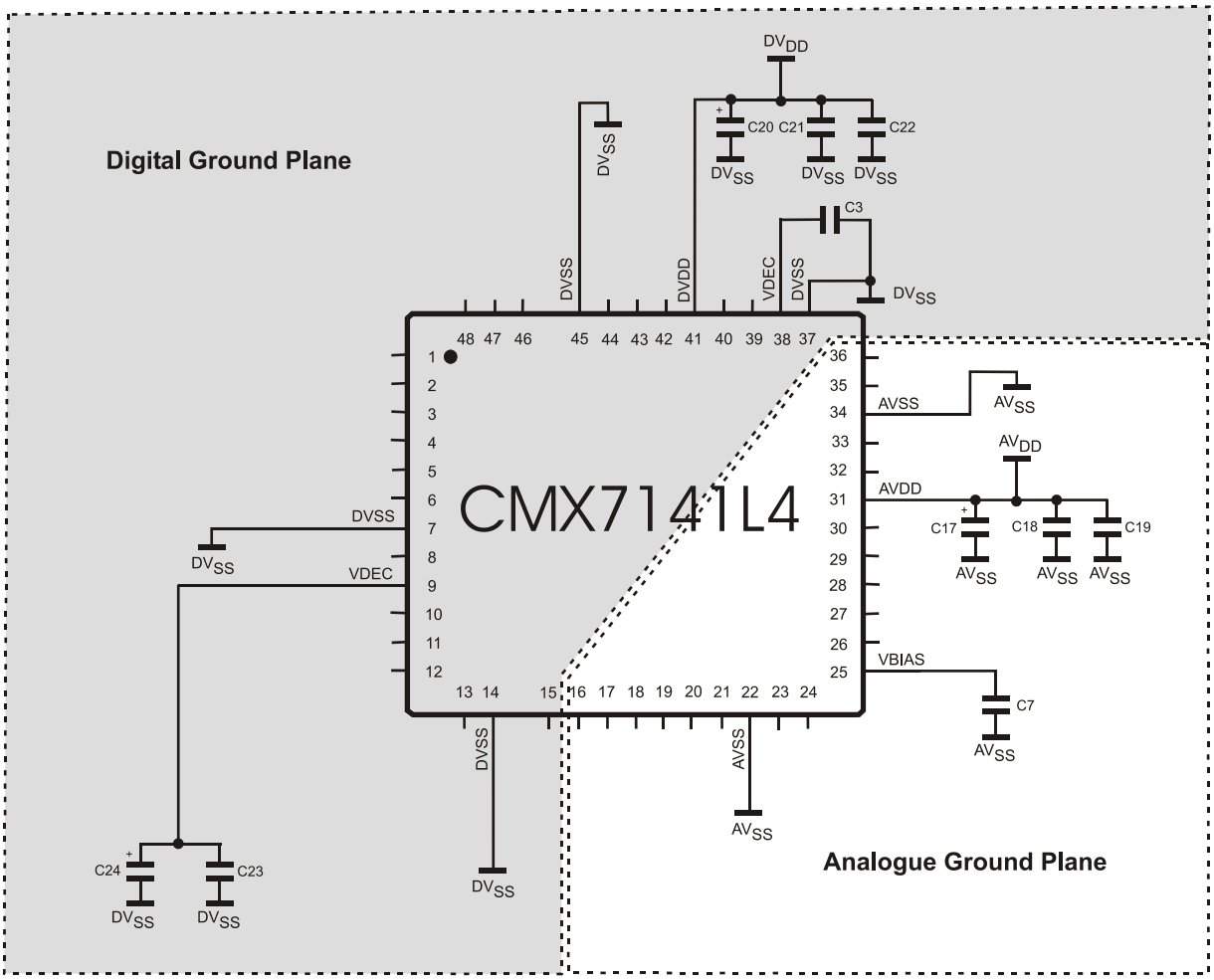


Figure 4 CMX7141 (L4/Q3) Power Supply and De-coupling
Component Values as per Figure 2

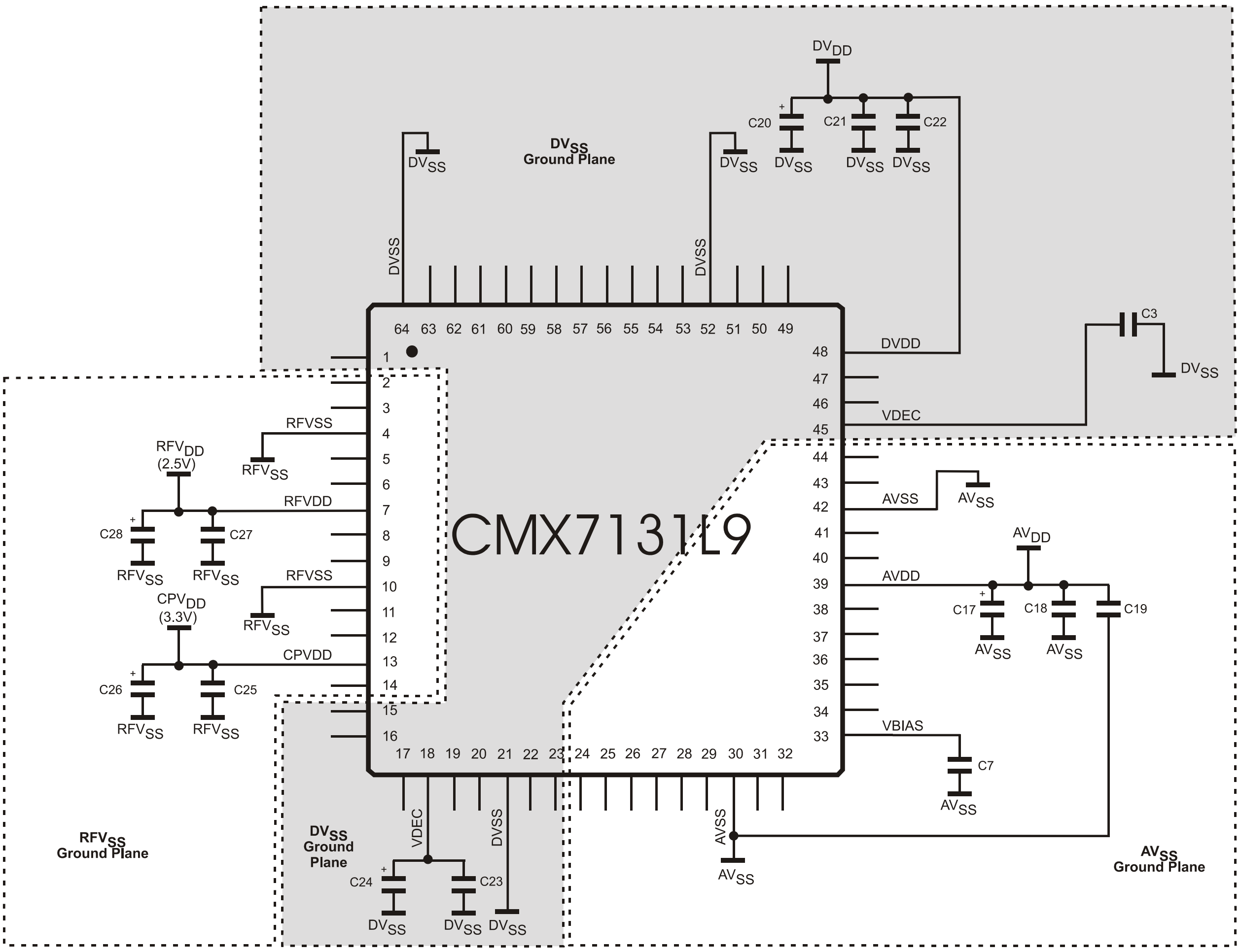


Figure 5 CMX7131 (L9/Q1) Power Supply and De-coupling

Component Values as per Figure 3

Notes:

It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the CMX7131/CMX7141 and the supply and bias de-coupling capacitors. The de-coupling capacitors C3, C7, C18, C19, C21, C22 and C24 should be as close as possible to the CMX7131/CMX7141. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS} and DV_{SS} supplies in the area of the CMX7131/CMX7141, with provision to make links between them, close to the CMX7131/CMX7141. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity. If V_{BIAS} is used to set the input mid-point reference, it should be buffered with a high input impedance buffer although the I/Q interface circuit of Figure 6 is permissible.

The single ended microphone input and audio output must be ac coupled (as shown), so that their return paths can be connected to AV_{SS} without introducing dc offsets. Further buffering of the audio output is advised.

The crystal, X1, may be replaced with an external clock source.

4.3 Recommended External Components (CMX994 Interface)

When operating the 7131/7141FI-8.0.x.x (I/Q mode) the interface to the CMX994 shown in Figure 6 should be used. Component values are shown in Table 3. Where values are not shown refer to the CMX994 datasheet. See also section 5.2.9.

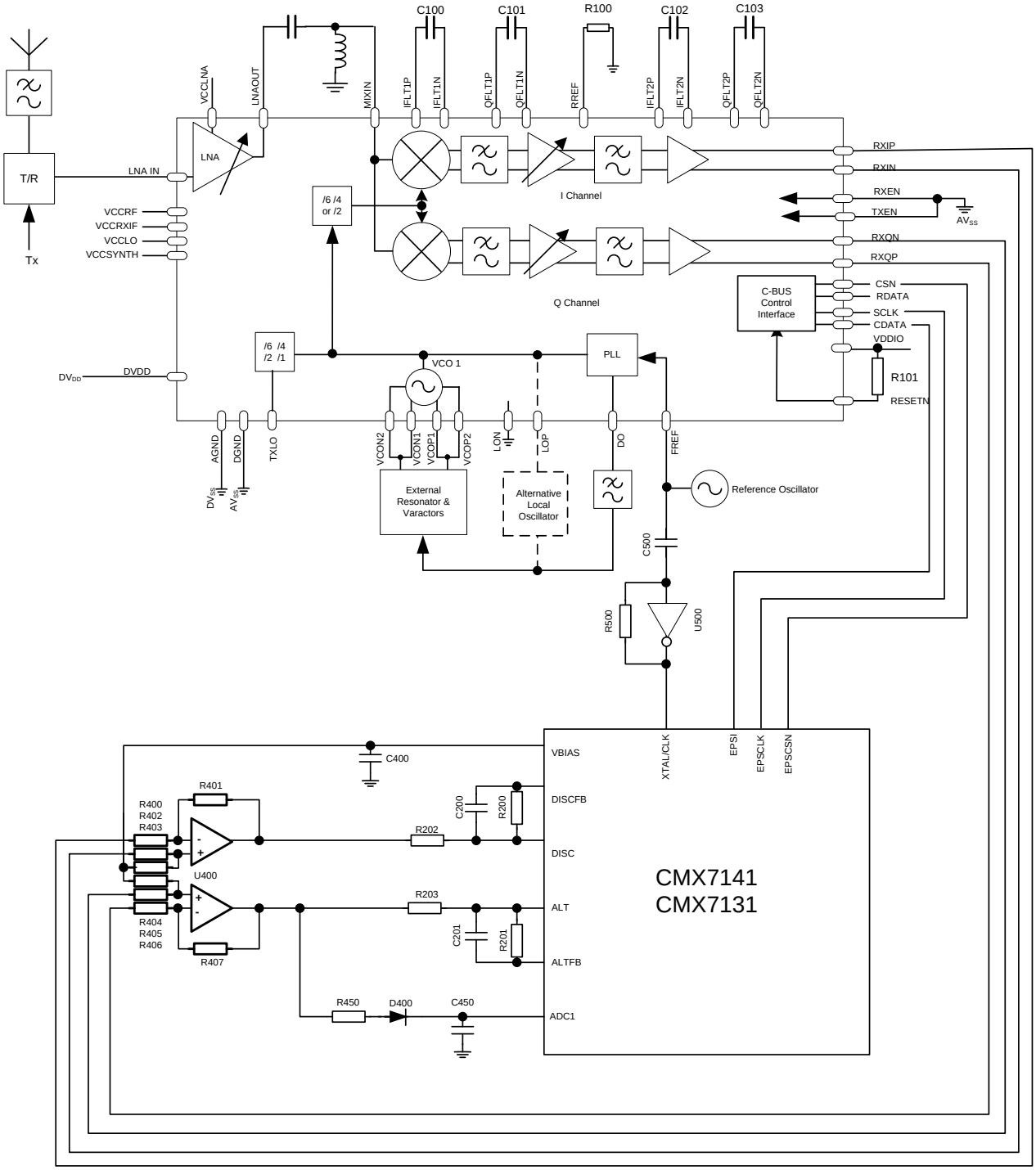


Figure 6 CMX994 Interface

Table 3 Recommended External Components when using CMX994

R100	10kΩ	C100	1.5nF	D400	MMBD1503A
R101	100kΩ	C101	1.5nF		
R200	100kΩ	C102	3.9nF	U400	e.g. LM6132
R201	100kΩ	C103	3.9nF	U500	e.g. SN74AHC1G04DRL
R202	100kΩ	C201	100pF		
R203	100kΩ	C202	100pF		
R400 to R407	10kΩ	C400	100nF		
R450	22 kΩ	C450	3.3pF		
R500	100kΩ	C500	1nF		

5 General Description

5.1 7131/7141FI-8.0.x.x Features

The 7131/7141FI-8.0.x.x Function Image™ is intended for use in half duplex analogue PMR equipment using 12.5 kHz or 25 kHz channels.

Much of the analogue signal processing required for EN 300 086 / EN 300 296 and TIA-603-Compliance is embedded in the 7131/7141FI-8.x Function Image™ operation namely:

Voice Processing:

- Pre/de-emphasis
- Audio channel filtering
- 300Hz high pass filter
- Voice companding
- Voice scrambling
- Voice AGC

Sub-Audio Signalling:

- CTCSS encode and decode (with CTCSS tone phase reversal)
- DCS encode and decode

In-Band Signalling:

- Selcall encode and decode
- 1200 bps FFSK modem
- DTMF encode and decode

The 7131/7141FI-8.x implements I/Q receiver mode and is tailored for operation with the CMX994 Direct Conversion Receiver IC. The transmitter circuits provide either a conventional output suitable for 2-point modulation or the signal in an I/Q format. A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals. The device includes a crystal clock generator, with buffered output, to provide a common system clock if required.

A block diagram of the device is shown in Figure 1. The signal processing blocks can be routed from any of the three DISC/ALT/MIC input pins (note: internal signal Input 1 must be connected to the receiver I channel and internal signal Input 2 must be connected to the receiver Q channel whichever of the DISC/ALT/MIC input stages are used (see register $B1).

Auxiliary Functions:

- Two programmable system clock outputs
- Two auxiliary ADCs with four selectable external input paths
- Four auxiliary DACs, one with built-in programmable RAMDAC
- Two RF PLLs (CMX7131 only)

Interface:

- Optimised C-BUS (4-wire high-speed synchronous serial command/data bus) interface to host for control and data transfer
- TXENA and RXENA hardware signals
- Open drain IRQ to host
- Two GPIO pins
- C-BUS (host) boot mode
- Auxiliary C-BUS interface to CMX994 Direct Conversion Receiver

5.2 System Design

5.2.1 Microphone

A microphone may be connected directly to the MIC input, which is configured as a differential amplifier with the positive input tied to VBIAS. This allows the gain and frequency response to be set by selecting appropriate values of C15, C16 and R9, R10. The device includes a programmable gain stage which can either be set by the host by writing to the Analogue Gain register ($B0) or can be left for the device to control as part of the Voice AGC functionality.

5.2.2 Speaker

A speaker amplifier may be connected to the AUDIO output pin. The signal level on this pin can be controlled using the Analogue Gain Register ($B0).

5.2.3 Modulation

Two separate modulation outputs are provided (MOD1, MOD2) with independent level controls to facilitate 2-point modulation systems. Alternatively, the same outputs may be configured to drive an I/Q modulator. In I/Q mode the modulation level is set to a maximum frequency deviation of 2.5kHz in order to be compatible with 12.5kHz channel operation. I/Q Tx mode is not suitable for 25kHz channel operation.

5.2.4 Audio / Voice processing

All the necessary processing blocks to support analogue FM voice for 12.5kHz or 25kHz channel operation are provided to support ETSI EN 300 086 / EN 300 296 and TIA-603 compatible systems. This includes:

- 300Hz HPF to reject sub-audio signalling
- Pre-emphasis and de-emphasis
- Channel filtering for 12.5kHz or 25kHz channels
- Programmable limiter (works in conjunction with the Voice AGC)

In addition, a frequency inversion voice scrambler and a voice compander are also provided.

The analogue signal levels must be set so as not to overload the internal processing blocks. In particular, pre-emphasis and de-emphasis processing will boost signals by up to 10dB, depending on their frequency. Threshold levels for the Voice AGC and Tx Limiter functions are host programmable.

5.2.5 Sub-audio Signalling

A 51-tone CTCSS and 83 code DCS encoder / decoder is provided which meets the requirements of TIA-603. Reverse Tone Burst and Squelch Tail Elimination are supported.

5.2.6 In-band Signalling

A fully flexible Selcall Tone encoder/decoder with host-programmable tones is provided. By default, the CCIR tone set is enabled. A 1200bps FFSK modem that meets the requirements of MPT1327 is available. This provides simultaneous detection of up to four different sync sequences, all of which are host programmable. A DTMF encoder/decoder is available. A general purpose audio tone generator is also available for generating “ring-tones”, confidence tones or key beeps etc.

5.2.7 RSSI and Squelch Measurement

The CMX7131/CMX7141 monitors the received signal in order to provide RSSI and Squelch values to the host. An interrupt can be generated based on RSSI or squelch level.

5.2.8 Serial Memory Connection

The auxiliary C-BUS/SPI-Codec bus is used in CMX7131/CMX7141FI-8.x for the CMX994 interface.

5.2.9 CMX994 Connection

The CMX994 should be connected via the auxiliary C-BUS connection (Table 4).

Table 4 CMX994 Connections

CMX7131/CMX7141 Pin	CMX994 pin
EPSCSN	CSN
EPSI	CDATA
EPSCLK	SCLK
No connection	RDATA

The operation of the CMX994 is generally automatic, however specific data may be written to CMX994 registers using the pass-through mode available using register $C8. For example, if the CMX994 PLL and VCO are used in the radio design then it is necessary to programme the appropriate frequency data to the CMX994 PLL -M Divider, PLL N-Divider and VCO Control registers using the pass-through mode before attempting reception. Operation of the CMX994 requires both BOOTEN pins to be permanently tied high.

CMX7131/CMX7141FI-8.x automatically controls the signal level and dc offset settings of the CMX994, providing an overall AGC, and can also implement an automatic powersave cycle.

5.2.10 Internal Data Processing

The CMX7131/CMX7141 operates as a half-duplex device, either receiving signals from the RF circuits in Rx mode, or sourcing signals to the RF circuits in Tx mode. It also has a low-power Idle mode. The internal data processing blocks for Tx and Rx modes are illustrated in Figure 7. The 7131/7141FI-8.x includes advanced features to automatically manage dc offset removal from the I/Q signals and optimise received signal quality.

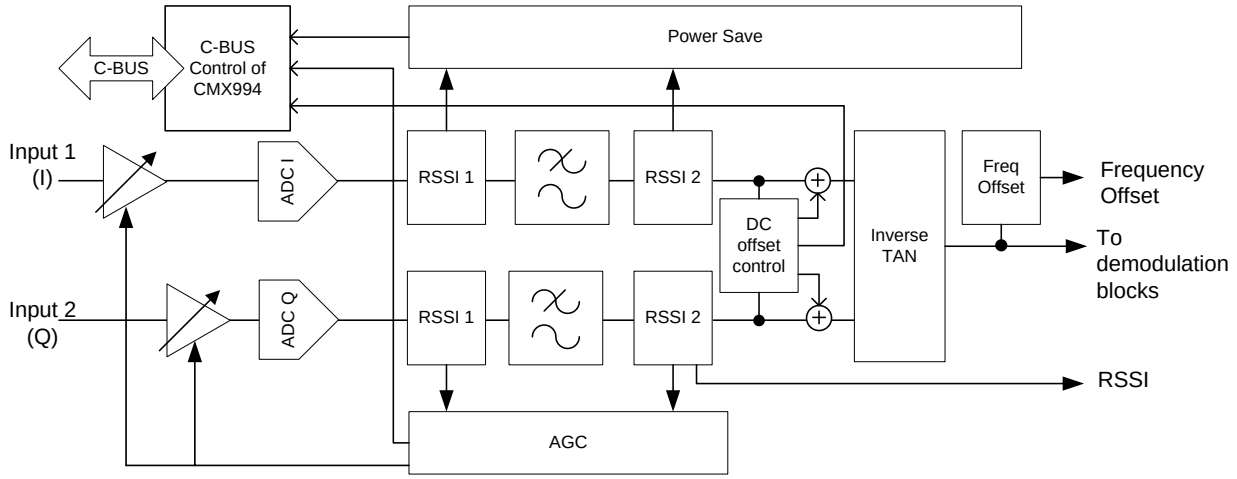


Figure 7 Internal I/Q Processing

5.2.11 Demodulation

The analogue signal from the receiver may be from a CMX994 I/Q interface or equivalent. The signal from the RF section should be applied to the CMX7131/CMX7141 inputs (normally the DISC and ALT inputs). See also section 6.16.1.

Filtering is applied to the input signals and dc offsets are removed before an inverse tan function performs FM demodulation. The output of this stage has an offset depending on the frequency error of the received signal compared to the nominal frequency of the receiver. This offset is removed before being passed to the analogue processing blocks. The device provides measurements of frequency error and RSSI.

5.2.12 Radio Performance Requirements

The recommended interfacing to the CMX994 should be used, see sections 4.3 and 5.2.9. The CMX7131/CMX7141 includes digital filters to provide adjacent channel rejection while compensating for the in-band response of the CMX994 I/Q filters.

For typical performance information see section 6.16.

6 Detailed Descriptions

6.1 Xtal Frequency

The CMX7131/CMX7141 is designed to work with an external frequency source of 19.2MHz. If this default configuration is not used, then Program Register Block 3 must be loaded with the correct values to ensure that the device will work to specification with the user-selected clock frequency.

A table of common values can be found in Table 5. Note the maximum Xtal frequency is 12.288MHz, although an external clock source of up to 24MHz can be used.

The register values in Table 5 are shown in hex, the default settings are shown in bold and the settings which do not give an exact setting (but are within acceptable limits) are in italics. The new P3.2-3 settings take effect following the write to P3.3 (the settings in P3.4-7 are implemented on a change to Rx or Tx mode).

Table 5 Xtal/Clock Frequency Settings for Program Block 3

Program Register			External Frequency Source (MHz)							
			3.579	6.144	9.216	12.0	12.8	16.368	16.8	**19.2**
P3.2	Idle	GP timer	*$017*	$018	$018	$019	$019	*$018*	$019	**$018**
P3.3	Idle	VCO output and AUX clk divide	*$085*	$088	$08C	*$10F*	*$110*	*$095*	*$115*	**$099**
P3.4	Rx or Tx	Ref clk divide	*$043*	$040	$060	$07D	$0C8	$155	$15E	**$0C8**
P3.5	Rx or Tx	PLL clk divide	*$398*	$200	$200	$200	$300	$400	$400	**$200**
P3.6 Note 1	Rx or Tx	VCO output and AUX clk divide	*$140*	$140	$140	$140	$140	$140	$140	**$140**
P3.7	Rx or Tx	Internal ADC/DAC clk divide	*$008*	$008	$008	$008	$008	$008	$008	**$008**

Note 1:

If the internal CTCSS/DCS or ACR AGC functions are used, the value of P3.6 MUST be changed to $0C0, which increases the internal processing speed by a factor two. As a consequence of this the RAMDAC speeds will also increase by the same amount. It is only necessary to write this data once following successful activation of the device.

6.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7131/CMX7141 and the host µC; this interface is compatible with microwire and SPI. Interrupt signals notify the host µC when a change in status has occurred and the µC should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 6.8.2.

The CMX7131/CMX7141 will monitor the state of the C-BUS registers that the host has written-to every 250µs (the C-BUS latency period). Hence the host should not make successive writes to the same C-BUS register within this period.

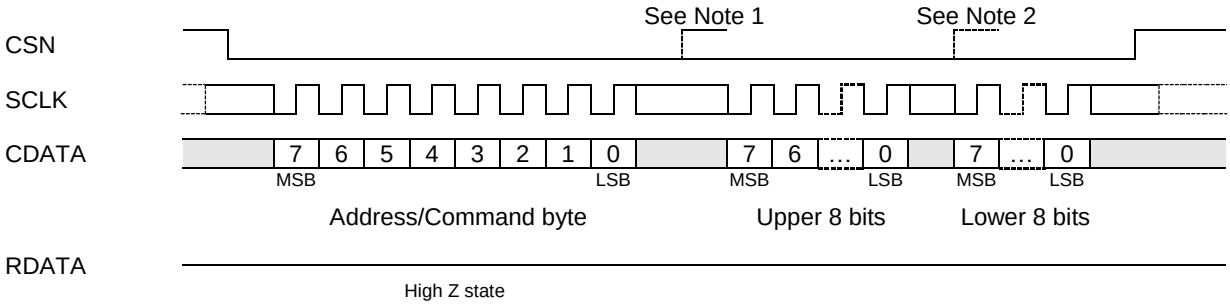
6.2.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX7131/CMX7141's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single address byte sent from the µC which may be followed by one or more data byte(s) sent from the µC and written to one of the CMX7131/CMX7141's Write Only registers, or one or more data byte(s) read from one of the CMX7131/CMX7141's Read Only registers, as shown in Figure 8.

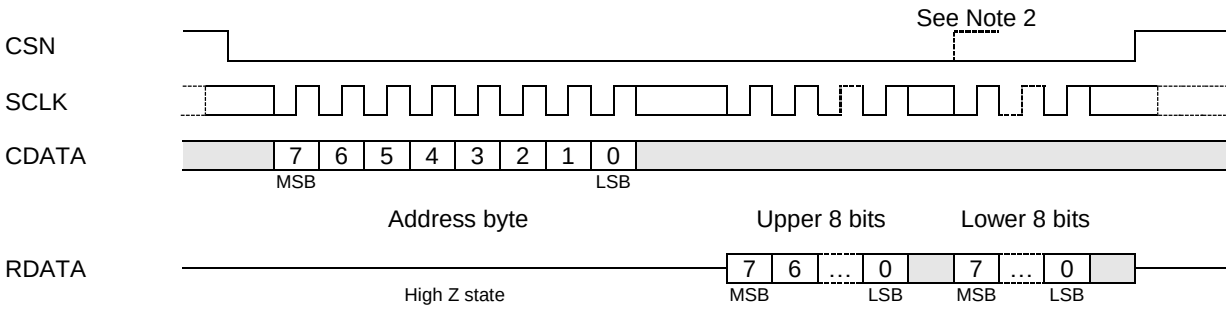
Data sent from the µC on the CDATA (Command Data) line is clocked into the CMX7131/CMX7141 on the rising edge of the SCLK (Serial Clock) input. RDATA (Reply Data) sent from the CMX7131/CMX7141 to the µC is valid when the SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an address byte is dependent on the value of the Address byte. The most significant bit of the address or data is sent first. For detailed timings see section 7.2. Note that, due to internal timing constraints, there may be a delay of up to 250µs between the end of a C-BUS write operation and the device reading the data from its internal register.

C-BUS Write:



C-BUS Read:



Data value unimportant

Repeated cycles

Either logic level valid (and may change)

Either logic level valid (but must not change from low to high)

Figure 8 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

6.3 Function Image™ Loading

NOTE: FI loading from serial memory is not supported with FI-8.x.

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file which must be included in the host controller software. The maximum possible size of Function Image™ is 46 kbytes, although a typical FI will be less than this. Note that the BOOTEN pins are read at power-on or following a C-BUS General Reset and must remain stable throughout the FI loading process. If the CMX994 is to be used with the CMX7131/CMX7141, then both BOOTEN pins should be pulled high permanently[2].

The BOOTEN pins are both fitted with internal low current pull-down devices.

For C-BUS load operation, both pins should be pulled high by connecting them to DV_{DD} either directly or via a 220kΩ resistor (see Figure 9).

Once the FI has been loaded, the CMX7131/CMX7141 performs these actions:

(1) The product identification code ($7141 or $7131) is reported in C-BUS register $C5
(2) The FI version code is reported in C-BUS register $C9
(3) The two 32-bit FI checksums are reported in C-BUS register pairs $A9, $AA and $B8, $B9
(4) The device waits for the host to load the 32-bit Device Activation Code to C-BUS register $C8
(5) Once activated, the device initialises fully, enters idle mode and becomes ready for use, and the PRG flag (bit 0 of the IRQ Status register) will be set.

The checksums should be verified against the published values to ensure that the FI has loaded correctly. Once the FI has been activated, the checksum, product identification and version code registers are cleared and these values are no longer available. If an invalid activation code is loaded, the device will report the value $DEAD in register $A9 and must be power-cycled before an attempt is made to re-load the FI and re-activate.

Both the Device Activation Code and the checksum values are available from the CML Technical Portal.

Table 6 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS Host load	1	1
Reserved	1	0
Reserved	0	1
No FI load	0	0

Note: Following a General reset, reloading of the Function Image is strongly recommended.

6.3.1 FI Loading from Host Controller

The FI can be included into the host controller software build and should be downloaded into the CMX7131/CMX7141 at power-up over the C-BUS interface. The BOOTEN pins must be set to the C-BUS load configuration and the CMX7131/CMX7141 powered up, which places the device into Program Mode. The data can then be sent directly over the C-BUS to the CMX7131/CMX7141.

If the host detects a brownout, the BOOTEN state should be set to re-load the FI. A General Reset should then be issued and the appropriate FI load procedure followed.

Each time the Programming register, $C8, is written, it is necessary to ensure that the PRG flag (IRQ Status register ($C6, b0) has gone high before another write to $C8. The PRG flag going high confirms the write to the Programming register has been accepted. The PRG flag state can be determined by unmasking the interrupt (Interrupt Mask register, $CE, b0) or by polling the IRQ Status[3] register.

[2] The PE0002 Interface Card will attempt to pull these pins low after loading the FI, details of additional script code to enable CMX994 operation is available from CML customer support.

[3] Polling is not recommended in normal operation due to the additional C-BUS transactions involved.

The download time is limited by the clock frequency of the C-BUS, with a 5MHz SCLK, it should take less than 500ms to complete.

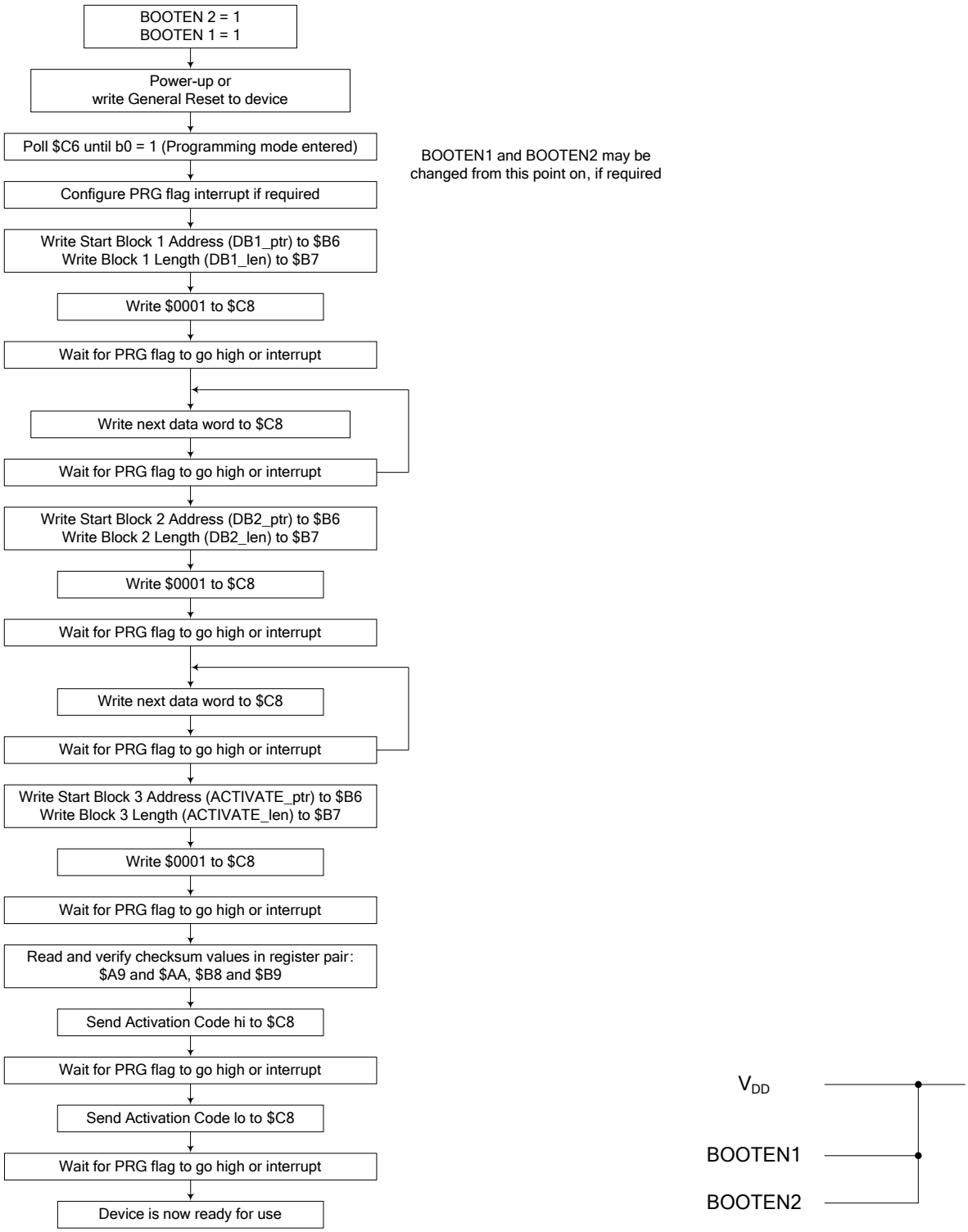


Figure 9 FI Loading from Host

6.4 Analogue PMR Description

6.4.1 Sub-Audio Processing

The filter used in the path can be set by the Program Register, P2.0, either a 260Hz Chebyshev suitable for CTCSS or a 150Hz 4-pole Bessel for DCS.

An internal generator/detector is available for the 51 CTCSS tones shown in Table 8 and the 83 DCS codes shown in Table 7. The tone/code to be generated is set by the value in the Analogue Mode register ($C2) in Tx mode and read from the Analogue Status read register ($CC) in Rx mode. See also the User Manual sections 8.1.23 and 8.1.32.

Squelch-tail elimination is provided by inverting the MOD outputs in CTCSS mode or a 134Hz “turn-off tone” in DCS mode. CTCSS tone phase reversal is detected and reported as Tone 253.

6.4.2 Voice Processing

A set of Audio Processing blocks is available for use in Analogue mode:

- 300Hz HPF
- 12.5kHz channel filter or 25kHz channel filter
- Hard limiter with anti-splatter filter
- Compander
- Frequency Inversion Scrambler
- Voice AGC
- Level adjust
- In–band audio generator/s in both Rx and Tx paths

The 12.5kHz channel filter (narrow) will be selected by default. the 25kHz filter (wide) can be enabled by setting P2.0:b0.

6.4.3 300Hz HPF

This is designed to reject signals below 300Hz from the voice path so that sub-audio signalling can be inserted (in Tx) or removed (in Rx) as appropriate. It should be enabled whenever sub-audio signalling is required.

6.4.4 12.5kHz/25kHz Channel Filters

These are designed to meet the requirements of ETSI EN 300 086 / EN 300 296 for voice signal processing and feature an upper roll-off at 2.55kHz. and 3.0kHz respectively

6.4.5 Hard Limiter

This is provided to limit the peak deviation of the radio signal to meet the requirements of ETSI EN 300 086 / EN 300 296. An anti-splatter filter is included to reduce the effects of any harmonic signals generated in the process. The limiter threshold can be set using P2.3.

6.4.6 Compander

A syllabic compressor/expander is provided, similar to that used in the 7031/7041-FI-1.x to increase the dynamic range of the Voice signal. The unity gain points for Tx and Rx can be set independently using P2.9 and P2.10.

6.4.7 Scrambler

A frequency inversion scrambler is provided to enable a basic level of privacy. The default inversion frequency is 3.3kHz, but can be programmed using $CD:$1001_b$, however some loss of signal at the band edges may occur due to the channel filter roll-off.

6.4.8 Voice AGC

An automatic gain control system is provided in the voice path, utilising the programmable gain settings of the Input 1 amplifier. When used in conjunction with the hard limiter function, this can compensate large variations in the MIC input signal without introducing significant distortion. The AGC threshold is

programmable using P2.1. whilst the maximum gain setting and the decay time can be set using P2.2. When this feature is enabled, the host should not attempt to directly control the Input 1 gain setting.

6.4.9 Level Adjust

Independent level adjustments are provided using the $C3 register for the voice, in-band and sub-audio signals as shown in Figure 10 and Figure 11.

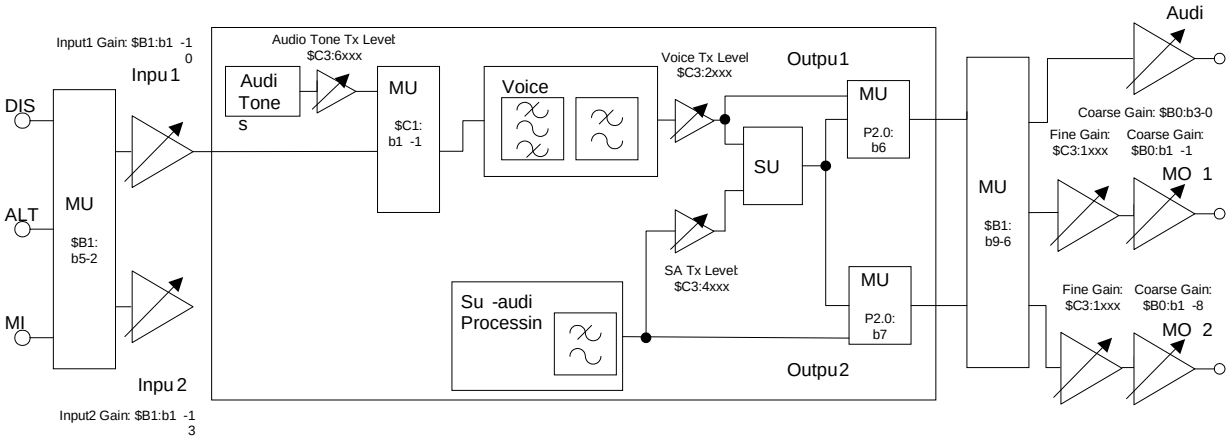


Figure 10 Tx Level Adjustments

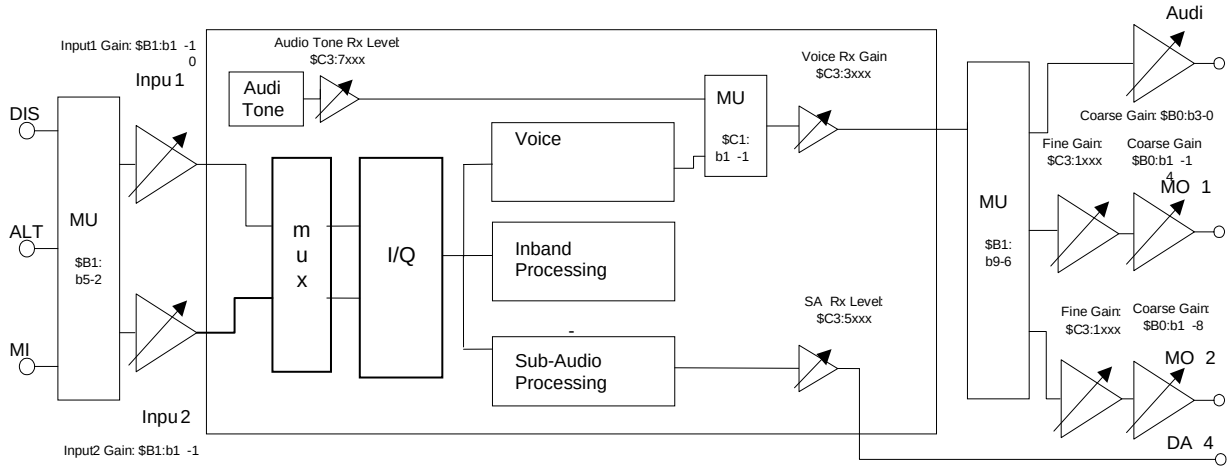


Figure 11 Rx Level Adjustments

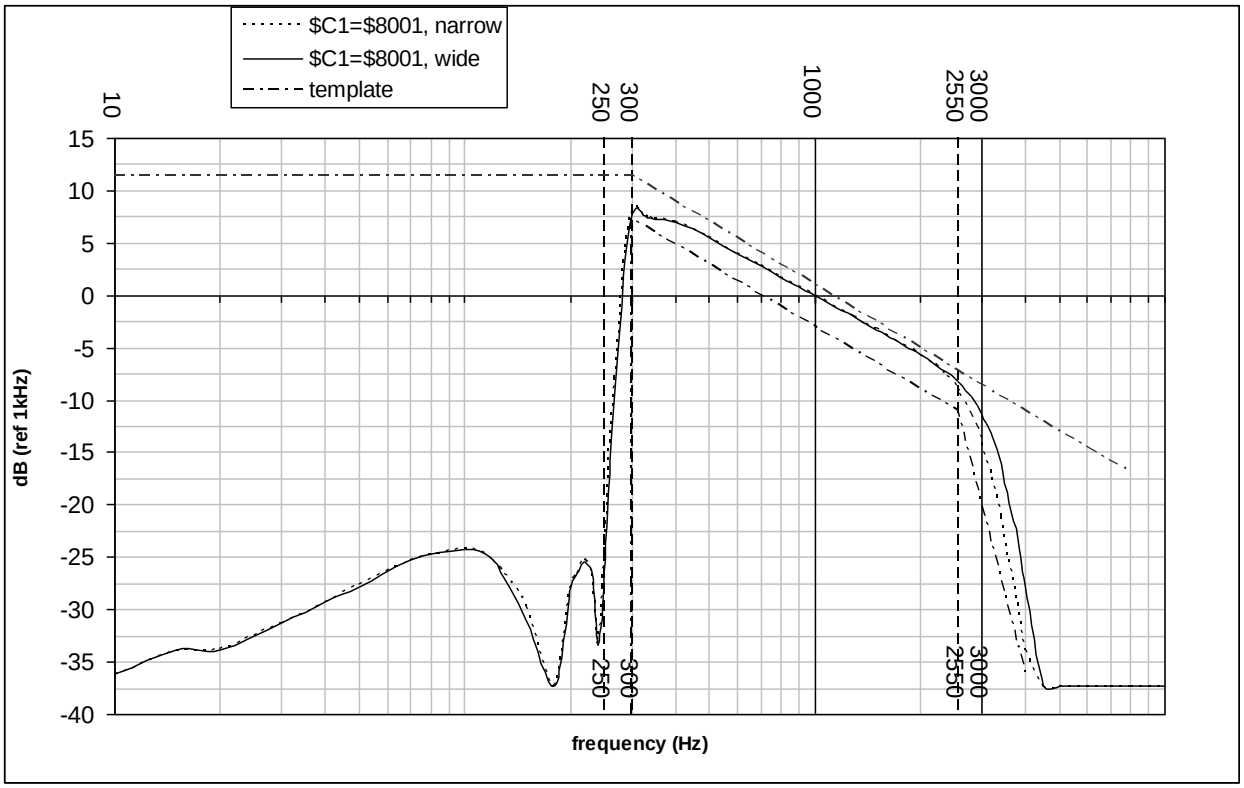


Figure 12 Rx Audio Response

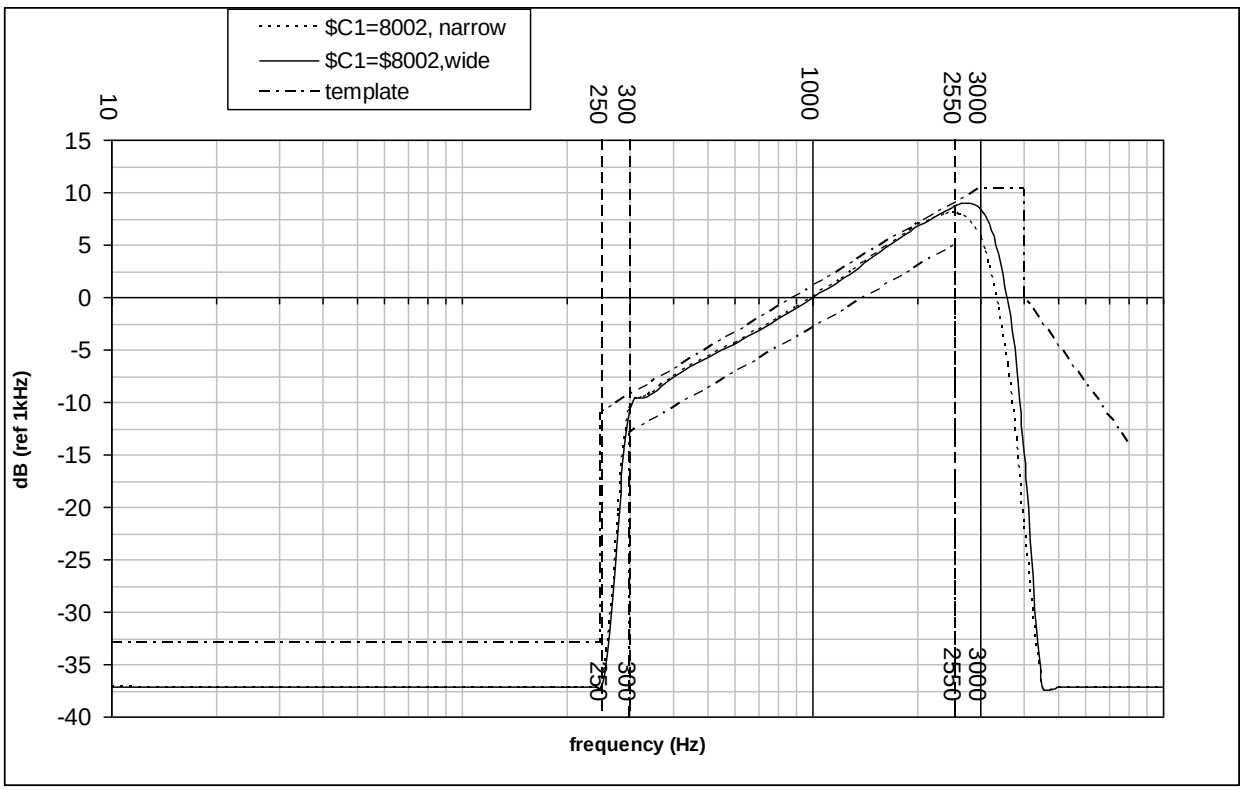


Figure 13 Tx Audio Response

Table 7 DCS Codes and Values

	Register Value			
DCS Code	**True**		**inverted**	
	Decimal	Hex	Decimal	Hex
no code	0	00	100	64
23	1	01	101	65
25	2	02	102	66
26	3	03	103	67
31	4	04	104	68
32	5	05	105	69
43	6	06	106	6A
47	7	07	107	6B
51	8	08	108	6C
54	9	09	109	6D
65	10	0A	110	6E
71	11	0B	111	6F
72	12	0C	112	70
73	13	0D	113	71
74	14	0E	114	72
114	15	0F	115	73
115	16	10	116	74
116	17	11	117	75
125	18	12	118	76
131	19	13	119	77
132	20	14	120	78
134	21	15	121	79
143	22	16	122	7A
152	23	17	123	7B
155	24	18	124	7C
156	25	19	125	7D
162	26	1A	126	7E
165	27	1B	127	7F
172	28	1C	128	80
174	29	1D	129	81
205	30	1E	130	82
223	31	1F	131	83
226	32	20	132	84
243	33	21	133	85
244	34	22	134	86
245	35	23	135	87
251	36	24	136	88
261	37	25	137	89
263	38	26	138	8A
265	39	27	139	8B
271	40	28	140	8C
306	41	29	141	8D

	Register Value			
DCS Code	**true**		**inverted**	
	Decimal	Hex	Decimal	Hex
311	42	2A	142	8E
315	43	2B	143	8F
331	44	2C	144	90
343	45	2D	145	91
346	46	2E	146	92
351	47	2F	147	93
364	48	30	148	94
365	49	31	149	95
371	50	32	150	96
411	51	33	151	97
412	52	34	152	98
413	53	35	153	99
423	54	36	154	9A
431	55	37	155	9B
432	56	38	156	9C
445	57	39	157	9D
464	58	3A	158	9E
465	59	3B	159	9F
466	60	3C	160	A0
503	61	3D	161	A1
506	62	3E	162	A2
516	63	3F	163	A3
532	64	40	164	A4
546	65	41	165	A5
565	66	42	166	A6
606	67	43	167	A7
612	68	44	168	A8
624	69	45	169	A9
627	70	46	170	AA
631	71	47	171	AB
632	72	48	172	AC
654	73	49	173	AD
662	74	4A	174	AE
664	75	4B	175	AF
703	76	4C	176	B0
712	77	4D	177	B1
723	78	4E	178	B2
731	79	4F	179	B3
732	80	50	180	B4
734	81	51	181	B5
743	82	52	182	B6
754	83	53	183	B7
user defined	84	54	184	B8

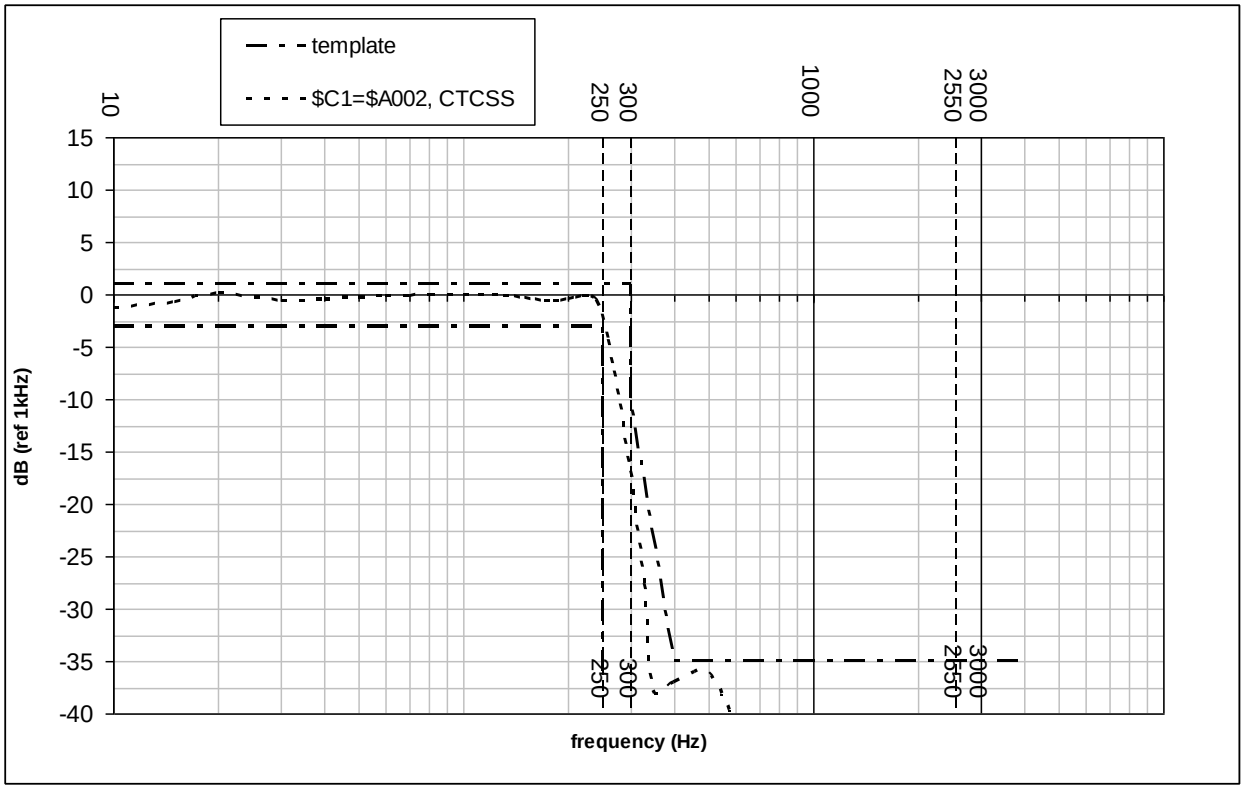


Figure 14 CTCSS Filter

Table 8 CTCSS Codes and Values

Register Value		CTCSS tone
Decimal	Hex	Frequency
200	C8	Tx: no tone Rx: Tone Clone
201	C9	67.0
202	CA	71.9
203	CB	74.4
204	CC	77.0
205	CD	79.7
206	CE	82.5
207	CF	85.4
208	D0	88.5
209	D1	91.5
210	D2	94.8
211	D3	97.4
212	D4	100.0
213	D5	103.5
214	D6	107.2
215	D7	110.9
216	D8	114.8
217	D9	118.8

Register Value		CTCSS tone
Decimal	Hex	Frequency
228	E4	173.8
229	E5	179.9
230	E6	186.2
231	E7	192.8
232	E8	203.5
233	E9	210.7
234	EA	218.1
235	EB	225.7
236	EC	233.6
237	ED	241.8
238	EE	250.3
239	EF	69.3
240	F0	62.5
241	F1	159.8
242	F2	165.5
243	F3	171.3
244	F4	177.3
245	F5	183.5

Register Value		CTCSS tone
Decimal	Hex	Frequency
218	DA	123.0
219	DB	127.3
220	DC	131.8
221	DD	136.5
222	DE	141.3
223	DF	146.2
224	E0	151.4
225	E1	156.7
226	E2	162.2
227	E3	167.9

Register Value		CTCSS tone
Decimal	Hex	Frequency
246	F6	189.9
247	F7	196.6
248	F8	199.5
249	F9	206.5
250	FA	229.1
251	FB	254.1
252	FC	user defined
253	FD	Phase Reversal
254	FE	DCS turn-off
255	FF	invalid tone

CTCSS detector thresholds and bandwidth are selectable using P2.4. Use of the “split tones” (239 to 251) will require a smaller bandwidth to be used, otherwise the adjacent tone frequency may be detected instead.

6.5 FFSK Data Modem

The device supports 1200 baud FFSK data mode suitable for use with MPT1327 or similar systems.

See:

- Mode Control - $C1 write
- Modem Configuration - $C7 write

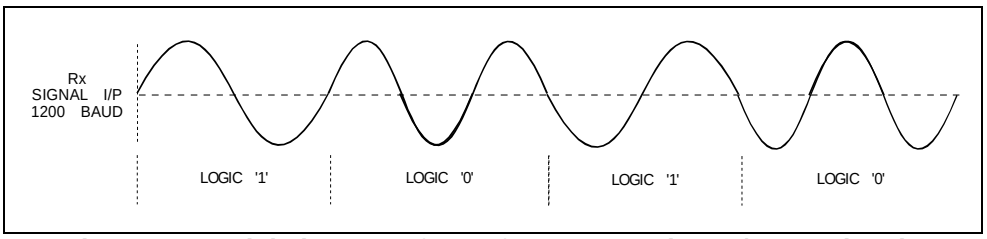


Figure 15 Modulating Waveforms for 1200 Baud MSK/FFSK Signals

The table below shows the combinations of frequencies and number of cycles to represent each bit of data.

Table 9 Data Frequencies for each Baud Rate

Baud Rate	Data	Frequency	Number of Cycles
1200baud	1	1200Hz	one
	0	1800Hz	one and a half

Note: FFSK may be transmitted in conjunction with a CTCSS or DCS sub-audio component.

6.5.1 Receiving FFSK Signals

The device can decode incoming FFSK signals at 1200 baud data rates. The form of FFSK signals is shown in Figure 15. A FFSK transmission begins with a preamble sequence followed by a 16 bit Sync sequence and then the user data.

The received signal is filtered and data is extracted with the aid of a PLL to recover the clock from the serial data stream. The recovered data is stored in a 2-byte buffer and an interrupt issued to indicate received data is ready. Data is transferred over the C-BUS under host µC control. If this data is not read before the next data is decoded it will be overwritten and it is up to the user to ensure that the data is transferred at an adequate rate following data ready being flagged. The FFSK bit clock is not output externally.

The extracted data is compared with the 16-bit programmed Frame Sync pattern (preset to $CB23 following a RESET command). An interrupt will be flagged when the programmed Frame Sync pattern is detected. The host µC may stop the frame sync search by disabling the FFSK demodulator. Once a valid Frame Sync pattern has been detected, the frame sync search algorithm is disabled; it may be re-started by the host disabling the FFSK bit of the Mode register ($C1:b8) and then re-enabling it (taking note of the C-BUS latency time).

Separate sync sequences are available, SynC, SynD, SynT and SynX. SynT is automatically derived as the inverse of the SynC sequence. All other sync sequences are user programmable. Sync detects are reported with an In Band event IRQ and a code in the Analogue Status register ($CC).

After frame synchronisation has been achieved, the user data which follows is made available in the RxData1 register. In an MPT1327 system, the SYS and CCS codes will also be reported in RxData3 and RxData4 (however, this is dependent on the timing of the signalling, the host should confirm the validity of the data before relying on it).

FFSK may be transmitted in conjunction with a CTCSS or DCS sub-audio component. The device will handle the sub-audio signals as previously described. If a sub-audio signal turns off during reception of FFSK, it is up to the host µC to turn off the decoding as the device will continue receiving and processing the incoming signal until commanded otherwise by the host µC.

The host µC must keep track of message length or otherwise determine end-of-reception (e.g. by using sub-audio information to check for signal presence) and disable the demodulator at the appropriate time.

6.5.2 Transmitting FFSK Signals

When enabled, the modulator will begin transmitting the preamble data (defined in P1.0), followed by the selected sync sequence (defined in P1.0 and selected by b11-8 of the Analogue Mode register ($C2). Therefore, these registers should be programmed to the required values before transmission is enabled.

The device will issue a DataRdy IRQ, which the host should respond to by loading the user data it wishes to transmit.

The device generates its own internal data clock and converts the binary data into the appropriately phased frequencies, as shown in Figure 15 and Table 9. The binary data is taken from TxData1 register ($CA), most significant bit first. The following data words must be provided over the C-BUS in response to the DataRdy IRQ. The end of the FFSK transmission may be indicated to the device by setting the TxData0 register to $0030, after which the device will indicate that the final data bit has left the chip by raising the TxDone IRQ, after which the host may power-down the RF circuitry and return the device to Idle mode as required.

6.6 Selcall Signalling

The device supports both Selcall and user-programmable Inband tones between 288Hz and 3000Hz. Note that if tones below 400Hz are used, sub-audio signalling should be disabled and the 300Hz HPF disabled.

By default, the device will load the EEA Selcall tone set, however this may be over-written by the host with any valid set of tones within its operational range by use of the Programming register. This ensures that the device can remain compatible with all available tone systems in use. The device does not implement automatic repeat tone insertion or deletion: it is up to the host to correctly implement the appropriate Selcall protocol.

Selection of the signalling mode is performed by bit 10 of the Mode register ($C1). Detection of the selected Inband signalling mode can be performed in parallel with voice reception.

See:

- Mode Control - $C1 write
- Analogue Mode - $C2 write
- TxData0 - $B5 write
- TxData1 - $B6 write
- Analogue Status - $CC read

6.6.1 Receiving and Decoding Selcall Tones

Selcall tones can be used to flag the start of a call or to confirm the end of a call. If they occur during a call the tone may be audible at the receiver. When enabled, an interrupt will be issued when a signal matching a valid inband tone changes state (ie: on, off or a change to different tone).

The device implements the EEA tone set. Other addressing and data formats can be implemented by loading the Programming registers with the appropriate values. The frequency of each tone is defined in the Programming registers P1.1 to P1.16.

In receive mode the device scans through the tone table sequentially. The code reported will be the first one that matches the incoming frequency and b3 of the IRQ Status register, $C6, will be asserted.

Adjustable decoder bandwidths and threshold levels are programmable via the Programming register. These allow certainty of detection to be traded against signal to noise performance when congestion or range limits the system performance.

Table 10 Inband Tones

Selcall Tones				
b12 - 8			Freq. (Hz)	Program Register
Binary	Dec	Hex		
00000	0	0	1981	P1.1
00001	1	1	1124	P1.2
00010	2	2	1197	P1.3
00011	3	3	1275	P1.4
00100	4	4	1358	P1.5
00101	5	5	1446	P1.6
00110	6	6	1540	P1.7
00111	7	7	1640	P1.8
01000	8	8	1747	P1.9
01001	9	9	1860	P1.10
01010	10	A	1055	P1.11
01011	11	B	930	P1.12
01100	12	C	2247	P1.13
01101	13	D	991	P1.14
01110	14	E	2110	P1.15
01111	15	F	2400	P1.16
10000	16	10	Null tone	-
11111	31	1F	Unknown tone	-

Notes:

1 Normally, tone 14 is the repeat tone. This code must be used in transmit mode when the new code to be sent is the same as the previous one. e.g. to send '333' the sequence '3R3' should be sent, where 'R' is the repeat tone. When receiving Selcall tones, the device will indicate the repeat tone when it is received. It is up to the host to interpret and decode the tones accordingly.

6.6.2 Alternative Selcall Tone Sets

These may be loaded via the Programming register to locations P1.1 to P1.16. See section 8.2.2.

Table 11 Alternative Selcall Tone Sets

	Frequency (Hz)				
Tone Number	**EIA**	**EEA**	**CCIR**	**ZVEI 1**	**ZVEI 2**
0	600	1981	1981	2400	2400
1	741	1124	1124	1060	1060
2	882	1197	1197	1160	1160
3	1023	1275	1275	1270	1270
4	1164	1358	1358	1400	1400
5	1305	1446	1446	1530	1530
6	1446	1540	1540	1670	1670
7	1587	1640	1640	1830	1830
8	1728	1747	1747	2000	2000
9	1869	1860	1860	2200	2200
A	2151	1055	2400	2800	885
B	2435	930	930	810	810
C	2010	2247	2247	970	740
D	2295	991	991	885	680
E	459	2110	2110	2600	970
F	NoTone	2400	1055	680	2600

6.7 DTMF Signalling

DTMF tone detection may be enabled in the Mode Control register ($C1) in parallel with other in-band Tone modes. When a DTMF tone has been detected, b14 of the Analogue Status register ($CC) and b3 of the IRQ Status register ($C6) will be set. This value will over-write any existing Inband tone value that may be present. The DTMF detector returns the values shown below in Table 12.

The DTMF signals to be generated are defined in the Tx Data1 register ($B6). The DTMF level is set using the Analogue Level register ($C3). Table 12 shows the DTMF tone pairs, together with the values for programming the 'Tone Pair' field of the Tx Data1 register ($B6). See also the User Manual sections 8.1.22, 8.1.15 and 8.1.24.

Table 12 DTMF Tone Pairs

Tone Code (Hex)	Key Pad Position	Low Tone (Hz)	High Tone (Hz)
1	1	697	1209
2	2	697	1336
3	3	697	1477
4	4	770	1209
5	5	770	1336
6	6	770	1477
7	7	852	1209
8	8	852	1336
9	9	852	1477
A	0	941	1336
B	*	941	1209
C	#	941	1477
D	A	697	1633
E	B	770	1633
F	C	852	1633
0	D	941	1633

6.8 Device Control

The CMX7131/CMX7141 can be set into the relevant mode to suit its environment. These modes are described in the following sections and are programmed over the C-BUS: either directly to operational registers or, for parameters that are not likely to change during operation, via the Programming register ($C8).

For basic operation:

1. Enable the relevant hardware sections via the Power Down Control register
2. Set the appropriate mode registers to the desired state
3. Select the required signal routing and gain
4. Use the Mode Control register to place the device into Rx or Tx mode.

To conserve power when the device is not actively processing a signal, place the device into Idle mode. Additional power saving can be achieved by disabling any unused hardware blocks. However, care must be taken not to disturb any sections that are automatically controlled by the FI. Note that the BIAS block must be enabled to allow any of the Input or output blocks to function.

See:

- Power Down Control - $C0 write
- Mode Control - $C1 write
- Modem Configuration - $C7 write.

6.8.1 General Notes

In normal operation the most significant registers are:

- Mode Control - $C1 write
- IRQ Status - $C6 read
- Analogue Output Gain - $B0 write
- Input Gain and Signal Routing - $B1 write
- Analogue Mode - $C2 write

Setting the Mode Control register to either Rx or Tx will automatically increase the internal clock speed to its operational value. Setting the Mode Control register to Idle will automatically return the internal clock to a lower (power-saving) speed. To access the Program Blocks (through the Programming register, $C8) the device MUST be in Idle mode. Under normal circumstances the CMX7131/CMX7141 manages the Main Clock Control automatically, using the default values loaded in Program Block 3.

6.8.2 Interrupt Operation

The CMX7131/CMX7141 will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the IRQ Status register and the IRQ Mask bit (bit 15) are both set to 1. The IRQ bit is set when the state of the interrupt flag bits in the IRQ Status register change from a 0 to 1 and the corresponding mask bit(s) in the Interrupt Mask register is(are) set. Enabling an interrupt by setting a mask bit ($0 \rightarrow 1$) after the corresponding IRQ Status register bit has already been set to 1 will also cause the IRQ bit to be set.

All interrupt flag bits in the IRQ Status register, except the PRG Flag (bit 0), are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the IRQ Status register. The PRG Flag bit is set to 1 only when it is permissible to write a new word to the Programming register.

See:

- IRQ Status - $C6 read
- Interrupt Mask - $CE write.

Continuous polling of the IRQ Status register ($C6) is not recommended due to both the increase in response time, host loading and potential digital noise generation due to bus activity. If the host cannot support a fully IRQ driven interface then it should route the IRQ signal to a host IO pin and poll this pin instead.

6.8.3 Signal Routing

The CMX7131/CMX7141 offers a flexible routing architecture, with three signal inputs, a choice of two modulator configurations (to suit two-point modulation or I/Q schemes) and a single audio output.

See:
- Input Gain and Signal Routing - $B1 write
- Mode Control - $C1 write
- Modem Configuration - $C7 write.

The analogue gain/attenuation of each input and output can be set individually, with additional Fine Attenuation control available via the Programming registers in the CMX7131/CMX7141.

See:
- Analogue Output Gain - $B0 write (MOD1 and 2)
- Input Gain and Signal Routing - $B1 write (DISC input, MOD1 and 2)

The internal signals Output 1 and Output 2 are used to provide either two-point or I/Q signals and should be routed to the MOD1 and MOD2 pins as required.

In Rx mode input 1 should be routed to the DISC input source for the I channel input and input 2 should be routed to the ALT input source for the Q channel input.

It is important to correctly configure the signal from the CMX994 I/Q outputs to the CMX7141 DISC and ALT inputs. Crossing these connections will cause the CMX7141 dc offset calibration to fail, as attempted corrections to the I signal will be made to the Q signal and vice versa. Crossed connections can be swapped using bits 2-5 of the Input Gain and Signal Routing register ($B1). Likewise, it is important that the polarity of connection is correct between the CMX994 and CMX7141. If the input signals are inverted then attempts by the CMX7141 to remove the dc offset will, in fact, increase the dc offset. The inputs may be inverted by using the 'Input Invert' bit (bit 7) in the Analogue Output Gain register ($B0). Often this can be corrected by swapping the I and Q signals (changing the signal that leads in phase to the one that lags). However, the relationship between I/Q outputs of the CMX994 and the CMX7141 DISC and ALT inputs must be maintained as described above. Therefore the demodulated signal can be inverted using Programming Register block 0, P0.10:b1 (IFD).

6.8.4 Modem Control

The CMX7131/CMX7141 operates in one of these operational modes:

- Idle (optionally with CMX994 pass-through)
- Rx (optionally with CMX994 control)
- Tx

At power-on or following a Reset, the device will automatically enter Idle mode, which allows maximum powersaving whilst still retaining the capability of monitoring the AuxADC inputs (if enabled).

(Note: To achieve minimum power consumption after Reset it is necessary disable the SYSCLK1 and SYSCLK2 outputs by writing $8000 to registers $AC and $AE, see section 6.14.2).

It is only possible to write to the Program Blocks whilst in Idle mode.

See:
- Mode Control - $C1 write.

GPIO1 and GPIO2 pins (RXENA and TXENA) reflect bits 0 and 1 of the Modem Control register, as shown in Table 13. These can be used to drive external hardware without the host having to intervene. There are also two additional GPIO pins that are programmable under host control.

Table 13 Modem Mode Selection

Modem Control ($C1) b3-0		Modem Mode	GPIO2 - TXENA	GPIO1 - RXENA
0	0000	Idle – Low Power Mode	1	1
1	0001	Rx	1	0
2	0010	Tx	0	1
3	0011	*Reserved*	x	x
4	0100	CMX994 Pass-through	1	1
5	0101	Rx with CMX994 I/Q cal	1	0
9	1001	Rx with Powersave	1	0
x	others	*Reserved*	x	x

6.8.5 Rx Mode

In Rx mode operation ($C1, Modem Control = $xxx1), the CMX7131/CMX7141 will automatically start searching for any of the enabled signalling modes. When a valid signal is detected, a 'Sub-audio' or 'In-band' detect' IRQ is asserted and the host should then examine the Analogue Status register ($CC) to determine the received data.

When receiving in I/Q Mode the CMX7131/CMX7141 will control its internal analogue gain and the gain of the CMX994 in order to keep the received I/Q signals within an acceptable dynamic range. This AGC feature may be disabled using Program Block P2.0:b11 (I/Q AGC function), in which case any setup that the host has made of the CMX994 will determine its gain, with the input gain of the CMX7131/CMX7141 being controlled using the Input Gain and Signal Routing - $B1 write register.

To improve the Adjacent/Alternate channel rejection performance, additional external circuitry (shown in Figure 6) can be connected to AuxADC1 and enabled by P2.0:b8. This consists of a filter and detector which is fed to the AuxADC1 input to ensure that signals outside the bandwidth of the device's main input path are taken into account when determining the AGC settings of the CMX994. This feature makes use of the AuxADC averaging and threshold settings and requires the internal processing speed to be increased to ensure accurate operation:

- P2.0 $E130 enable I/Q AGC, I/Q VAD, ACR AGC and Internal sub-audio
- P3.0 $F002 enable averaging setting = 2
- P3.6 $70C0 increase internal processing speed
- $A7 $0030 route AuxADC1 to ADC1 input pin
- $CD $4205 set hi threshold to $205
- $CD $0200 set lo threshold to $200

Notes:

The writes to the $CD register MUST observe the C-BUS latency time
Increasing the internal processing speed will also increase the RAMDAC speed
Values of P3.2 to P3.7 should be as shown in Table 5.

It is important to ensure that the dc offset on the I/Q signals is small, otherwise the AGC function will interpret the dc as a large received signal and never select maximum gain. This problem can be addressed by calibrating the CMX994 as described in Section 6.8.8.

6.8.6 Tx Mode

In Tx mode operation ($C1, Modem Control = $xxx2), the host should write the initial configuration to the Analogue Mode register ($C2) before placing the device into Tx.

6.8.7 CMX994 Pass-through Mode

To allow the host to communicate directly with the CMX994 for test and configuration purposes, a pass-through mode is available which allows any CMX994 C-BUS register to be written. This mode uses the TxData0 and Programming registers on the CMX7131/CMX7141.

To write to the CMX994:

1. Set the CMX7131/CMX7141 to CMX994 Pass-through mode ($C1=$0004)
2. Wait for the Program Flag to be set ($C6 b0)
3. Write the CMX994 data value to the TxData0 register ($B5)
4. Write the CMX994 C-BUS address to the Programming register ($C8) with b15-13=$011_2$
5. Wait for the Program Flag to be set ($C6 b0)
6. Repeat from 3 if required

See section 6.16 for further details of CMX994 operation.

6.8.8 Rx Mode with CMX994 I/Q Cal

When receiving, the CMX7131/CMX7141 will estimate and remove the dc error present in the I/Q signals from a CMX994 receiver. However, it is necessary to calibrate the CMX994 so that the magnitude of the dc offsets present is as small as possible. Selecting Rx mode with CMX994 I/Q Cal ($C1, Modem Control b3-0 = $5) causes the CMX7131/CMX7141 to measure the dc offset on the DISC and ALT input pins and to control the CMX994 receiver to minimise the dc offsets. The CMX7131/CMX7141 will then begin to receive normally – correcting the remaining dc offset internally.

Important note: when calibrating I/Q it is important that the I/Q signals are not swapped when interfacing to the CMX994. If hardware happens to be wired incorrectly the I/Q inputs to the signal processing can be swapped by using bits 2 to 5 of the Input Gain and Routing register ($B1).

If the CMX994 is poorly calibrated, a loss of headroom when receiving signals will result. In extreme cases, when large dc offsets are amplified, the result can be big enough to prevent the AGC from reaching maximum gain as it interprets the dc offset itself as a large signal.

Having calibrated the CMX994, the value written to the CMX994 dc offset correction register is available to read using the Aux Data and Status ($A9, $AA) registers. This means that, having calibrated the CMX994 on a receive channel the calibration result may be stored by the host microcontroller and restored at a later time.

6.8.9 Rx Mode with Powersave

Selecting powersave mode ($C1, Modem Control b3-0 = $xxx9) will cause the CMX7131/CMX7141 to control the CMX994, switching it into a low-power state for a period of time. Once the powersave timer has expired then the CMX994 and the internal circuits of the CMX7131/CMX7141 will be powered up, ready to receive.

On entering the powered up state, the CMX7131/CMX7141 will monitor the received I/Q signals for energy in its sampled bandwidth (threshold 1), and if there is no signal present it will return to the powersave state, powering down the CMX994. If sampled energy is found then the signal is passed through a channel filter and the resulting signal measured again (threshold 2) and if no signal is found the powersave state is selected once more. Finally a squelch measurement is taken, by FM demodulating the received signal and measuring the energy above the expected signal bandwidth. If squelch indicates (threshold 3) that the signal is a good signal, powersave mode is ended, leaving the CMX994 and CMX7131/CMX7141 on and in receive until the mode register is written to.

The three power save thresholds can be adjusted using the Aux Config register ($CD). The same register can be used to program the powersave off time. The values of the three measurements can be monitored duing a special test mode which can be selected from the Mode Control register ($C1) with b7-b4 = 0011_b.

In this mode, reading the following registers will return the measurement values:

$BA = input signal level (used for threshold 1)

$BB = signal level after channel filtering (used for threshold 2)

$C5 = squelch level (used for threshold 3)

The values returned in $BA and $BB correspond to the relevant thresholds set in $CD. The squelch threshold is different because here the signal is accumulated and the value being large indicates the presence of a valid signal. In this case the threshold set in $CD is left-shifted by 4 bits, so writing a value of $500 results in a threshold of $5000. This explains the scaling of numbers displayed in $C5.

Throughout the time that the receiver is on, the CMX7131/CMX7141 will search for a valid signal (CTCSS/DCS/Selcall/FFSK/DTMF) and start receiving the signal. However, dependent on the powersave period, it is possible that the frame sync at the start of a burst may be missed, in which case 'late entry' is possible.

Thresholds for comparison and timings for powersave mode may be adjusted, potentially improving powersaving by being powered down for a greater period of time, but at the expense of a slower reaction to received signal. See the Aux Config $CD write register.

Note: To achieve minimum power consumption it is necessary disable the SYSCLK1 and SYSCLK2 outputs by writing $8000 to registers $AC and $AE, see section 6.14.2.

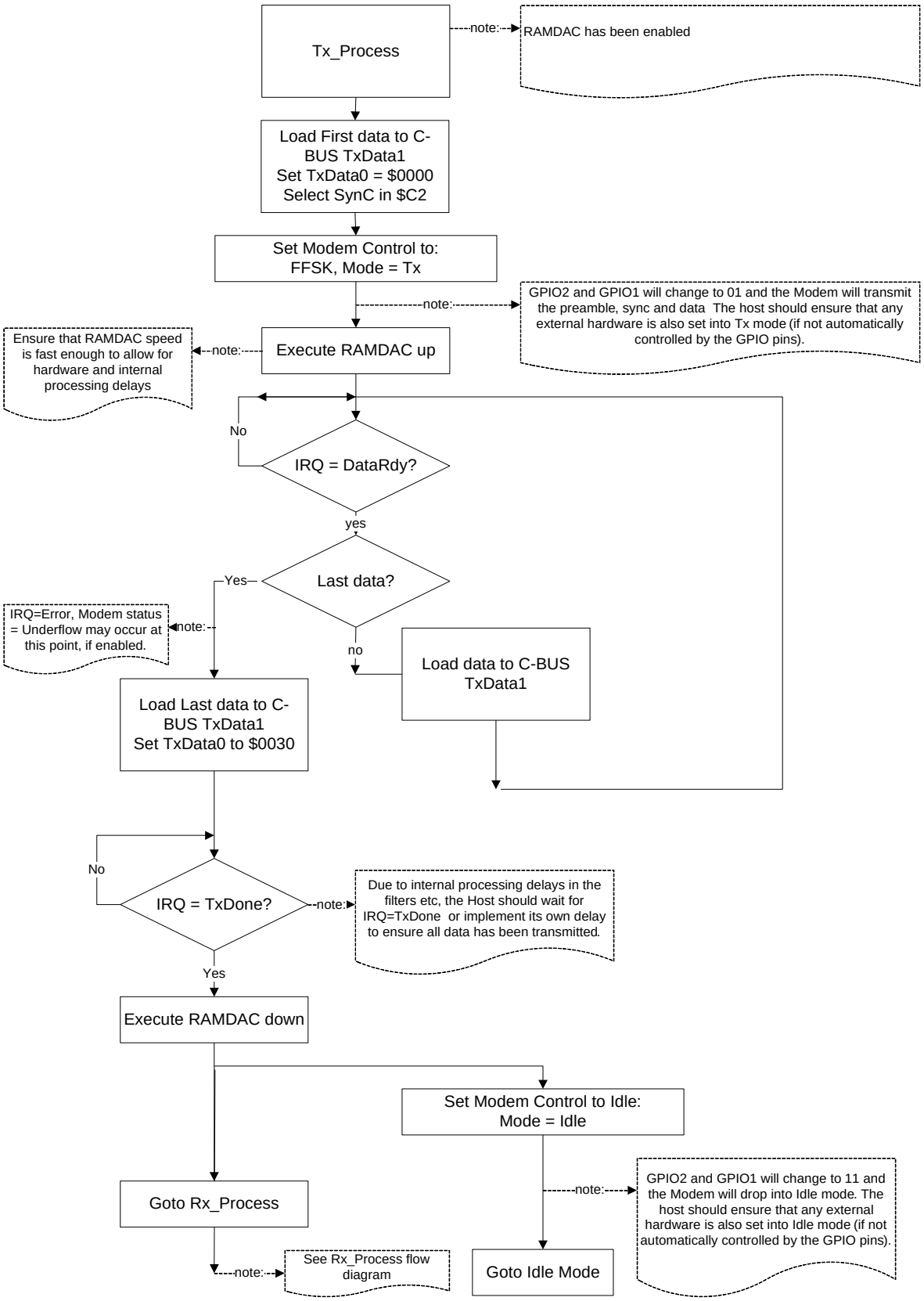


Figure 16 FFSK Tx Data Flow

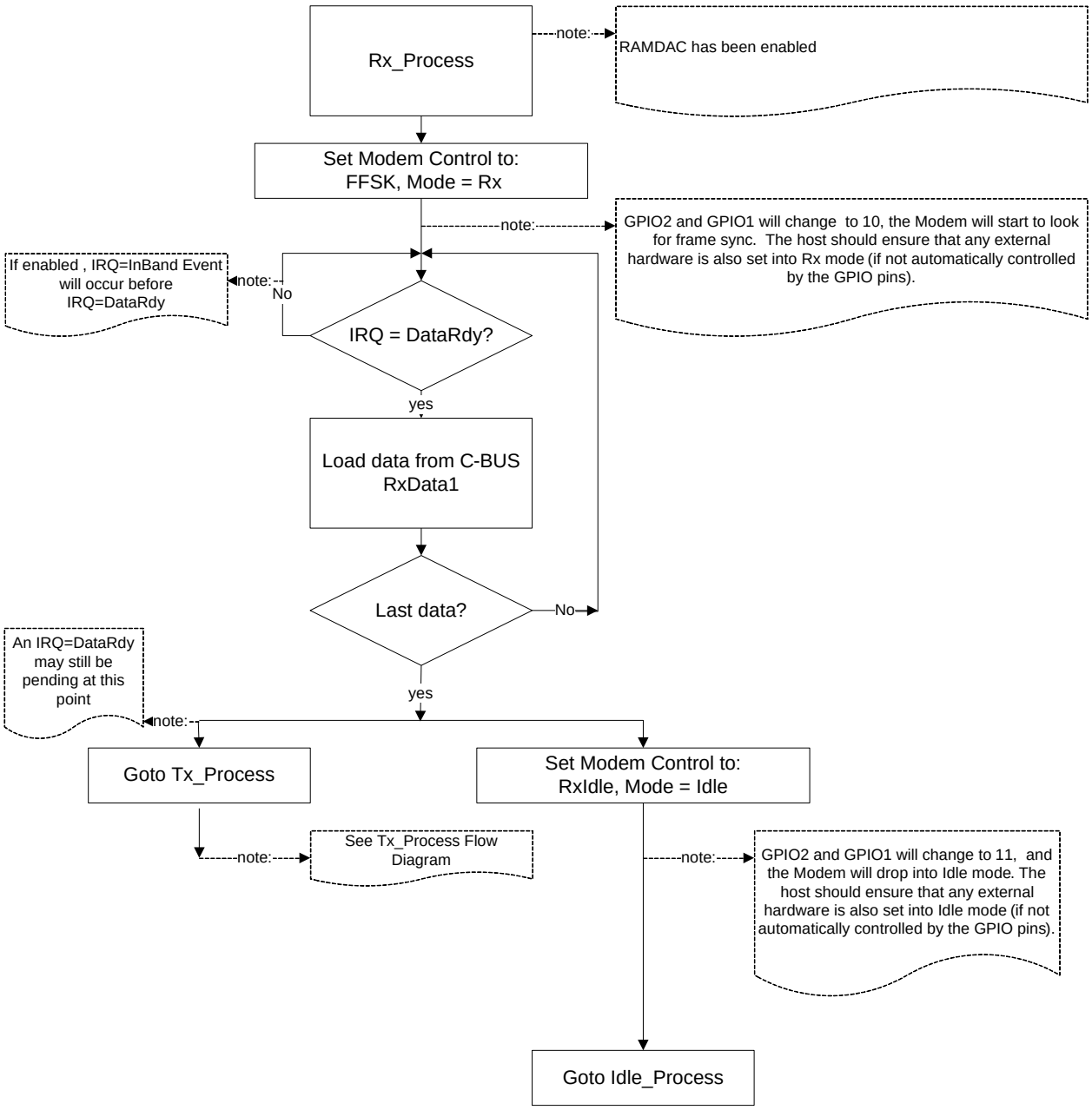


Figure 17 FFSK Rx Data Flow

See:

- RxData0 - $B8 read
- Analogue Status - $CC read.

6.9 Squelch Operation

Squelch detection is implemented within CMX7131/CMX7141 I/Q signal processing.

6.10 GPIO Pin Operation

The CMX7131/CMX7141 provides four GPIO pins: GPIO1, GPIO2, GPIOA and GPIOB. RXENA (GPIO1) and TXENA (GPIO2) are configured to reflect the Tx/Rx state of the Mode register (TXENA and RXENA, active low).

See:

- Modem Configuration - $C7 write.

Note that RXENA and TXENA will not change state until the relevant mode change has been executed by the CMX7131/CMX7141. This is to allow the host sufficient time to load the relevant data buffers and the CMX7131/CMX7141 time to encode the data required prior to its transmission. There is thus a fixed time delay between the GPIO pins changing state and the data signal appearing at the MOD output pins. During the power-on sequence (until the FI has completed its load sequence) these pins have only a weak pull-up applied to them, so care should be taken to ensure that any loading during this period does not adversely affect the operation of the unit.

GPIOA and GPIOB are host programmable for input or output using the AuxADC Configuration register, $A7. The default state is output, high level. When set for input, the values can be read back using the Modem Status register, $C9.

6.11 Auxiliary ADC Operation

The inputs to the two auxiliary ADCs can be independently routed from any of the signal input pins under control of the AuxADC Configuration register, $A7. Conversions will be performed as long as a valid input source is selected. To stop the ADCs, the input source should be set to 'off'. Register $C0, b6, BIAS, must be enabled for auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the AuxADC Configuration register, $A7, the length of the averaging is determined by the value in the Programming register (P3.0 and P3.1), and defaults to a value of 0. This is a rolling average system such that a proportion of the current data will be added to the last average value. The proportion is determined by the value of the average counter in P3.0 and P3.1.

For an average value of:

0 = 50% of the current value will be added to 50% of the last average value,
1 = 25% of the current value will be added to 75% of the last average value,
2 = 12.5% etc.

The maximum useful value of this field is 9.

High and Low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated when a rising edge passes the High threshold or a falling edge passes the Low threshold, see Figure 18. The thresholds are programmed via the Aux Config $CD write register. See Figure 18.

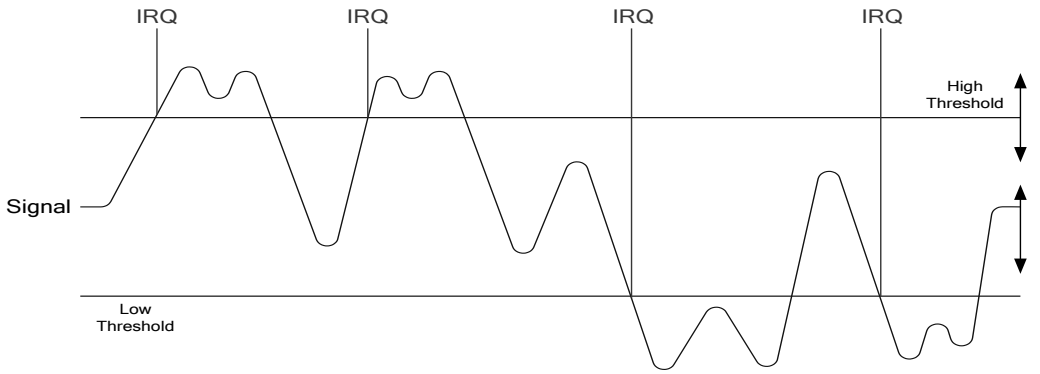


Figure 18 AuxADC IRQ Operation

Auxiliary ADC data is read back in the Aux 1 Data registers ($A9 and $AA) and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

See:
- AuxADC Configuration - $A7 write
- Aux 1 Data and Status - $A9 read
- Aux 2 Data and Status - $AA read
- Aux Config $CD write.

To improve the Adjacent/Alternate channel rejection performance, an additional external filter/detector circuit connected to AuxADC1 can be utilised. This mode is selected by setting P2.0:b8. In this mode ADC1 is no longer available for other functions.

6.12 Auxiliary DAC/RAMDAC Operation

The four auxiliary DAC channels are programmed via the AuxDAC Data/Control register, $A8. AuxDAC channel 1 may also be programmed to operate as a RAMDAC which will automatically output a pre-programmed profile at a programmed rate. The AuxDAC Data/Control register, $A8, with b12 set, controls this mode of operation. The default profile is a raised cosine (see Table 19), but this may be over-written with a user-defined profile by writing to Programming register P3.11. The RAMDAC operation is only available in Tx mode and, to avoid glitches in the ramp profile, it is important not to change to Idle or Rx mode whilst the RAMDAC is still ramping. The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero. Note that access to all four AuxDACs is controlled by the AuxDAC Data/Control register, $A8, and therefore to update all AuxDACs requires four writes to this register. It is not possible to simultaneously update all four AuxDACs.

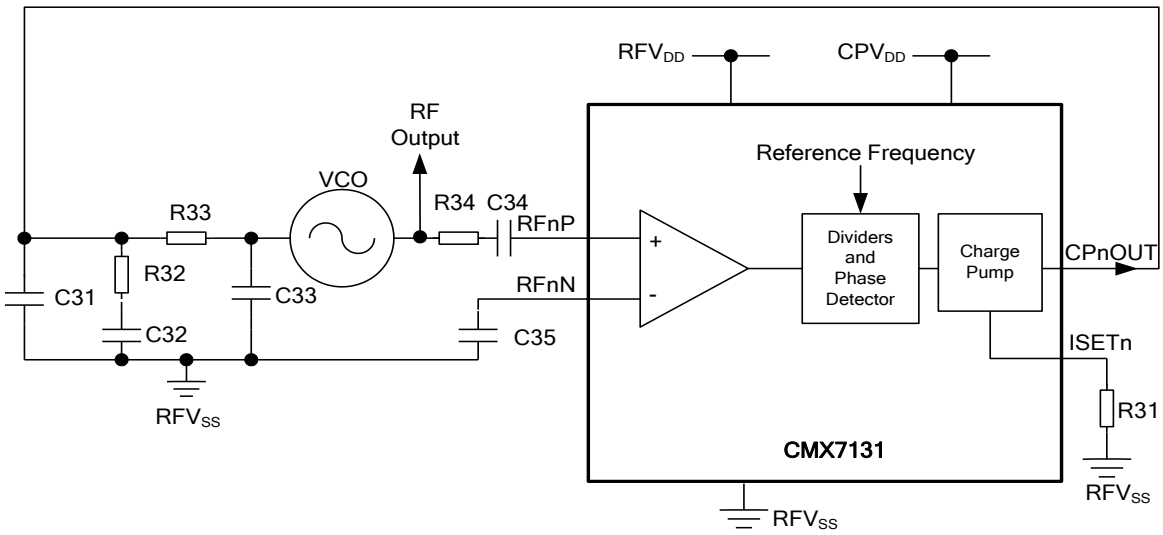
See:
- AuxDAC Data and Control - $A8 write.

6.13 RF Synthesiser (CMX7131 only)

The CMX7131 includes two Integer-N RF synthesisers, each comprising a divider, phase comparator and charge pump. The divider has two sets of N and R registers: one set can be used for transmit and the other for receive. The division ratios can be set up in advance by means of C-BUS registers. A single C-BUS command will change over from the transmit to the receive division ratios, or vice versa, enabling a fast turnaround.

See:
- RF Synthesiser Data - $B2 write
- RF Synthesiser Control - $B3 write
- RF Synthesiser Status - $B4 8-bit read.

External RF components are needed to complete the synthesiser circuit. A typical schematic for a 446MHz synthesiser (3.125kHz comparison frequency) is shown in Figure 19.



Note: n = 1 or 2 for Synthesiser 1 or 2

Figure 19 Example RF Synthesiser Components

R31	0Ω	C31	22nF
R32	5.6kΩ	C32	470nF
R33	10kΩ	C33	10nF
R34	100Ω	C34	1nF
		C35	1nF

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Note: R31 is chosen within the range 0Ω to 30kΩ and selects the nominal charge pump current.

It is recommended that C34 and C35 are kept close to the VCO and that the stub from the VCO to the CMX7131 is kept as short as possible. The loop filter components should be placed close to the VCO.

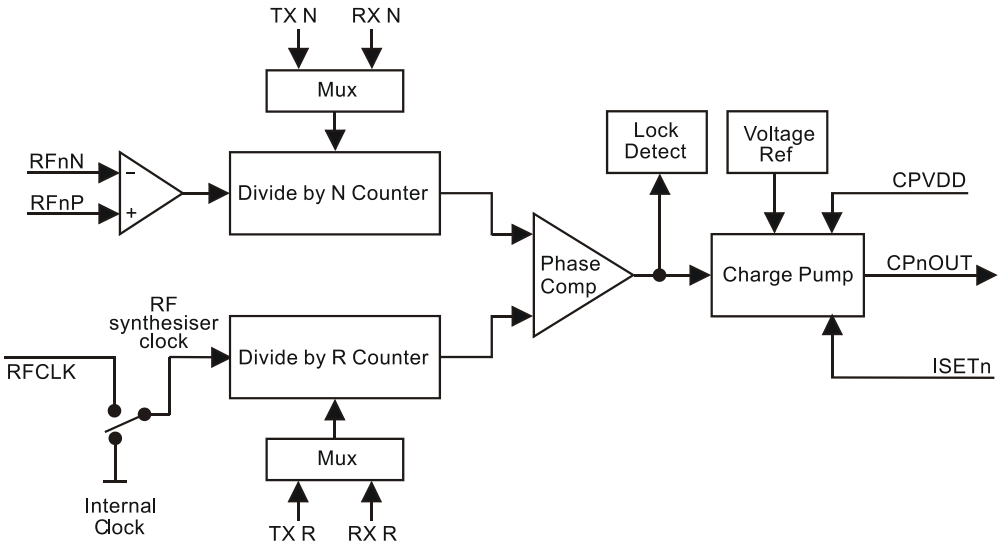


Figure 20 Single RF Synthesiser Block Diagram

The two RF synthesisers are programmable to any frequency in the range 100MHz to 600MHz. Figure 20 is a block diagram of one synthesiser channel. The RF synthesiser clock is selectable between the XTAL and the clock supplied to the RFCLK input pin. The RF synthesiser clock is common to both synthesisers. The charge pump supply (CP supply, CPVDD) is also common to both synthesisers. The RFnP and RFnN input pins, CPnOUT, ISETn and RFVSS pins are channel specific and designated as either RF1P, RF1N,

CP1OUT, ISET1, RFVSS or RF2P, RF2N, CP2OUT, ISET2, RFVSS on the Signal List in section 3. The N and R values for Tx and Rx modes are synthesiser specific and can be set from the host µC via the C-BUS. Various synthesiser specific status signals are also accessible via C-BUS. The divide by N counter is 20 bits; the R counter is 13 bits. Typical external components are shown in Figure 19.

Both synthesisers are phase locked loops (PLLs) of the same design, utilising external VCOs and loop filters. The VCOs need to have good phase noise performance although it is likely that the high division ratios used will result in the dominant noise source being the reference oscillator. The phase detectors are of the phase-frequency type with a high impedance charge pump output requiring just passive components in the loop filter. Lock detect functions are built in to each synthesiser and the status reported via C-BUS. A transition to out-of-lock can be detected and communicated via a C-BUS interrupt to the host µC. This can be important in ensuring that the transmitter cannot transmit in the event of a fault condition arising.

Two levels of charge pump gain are available to the user, to facilitate the possibility of locking at different rates under program control. A current setting resistor (R31) is connected between the ISET pin (one for each PLL system) and the respective RFVSS pin. This resistor will have an internally generated band gap voltage expressed across it and may have a value of 0Ω to 30kΩ, which (in conjunction with the on-chip series resistor of 9.6kΩ) will give charge pump current settings over a range of 2.5mA down to 230µA (including the control bit variation of 4 to 1). The value of the current setting resistor (R31) is determined in accordance with the following formulae:

gain bit set to 1: R31 (in Ω) = $(24/I_{CP}) – 9600$
gain bit cleared to 0: R31 (in Ω) = $(6/I_{CP}) – 9600$
where I_{CP} is the charge pump current (in mA).

Note that the charge pump current should always be set to at least 230µA. The ‘gain bit’ refers to either bit 3 or bit 11 in the RF Synthesiser Control register, $B3.

The step size (comparison frequency) is programmable; to minimise the effects of phase noise this should be kept as high as possible. This can be set as low as 2.5kHz (for a reference input of 20MHz or less), or up to 200kHz – limited only by the performance of the phase comparator.

The frequency for each synthesiser is set by using two registers: an ‘R’ register that sets the division value of the input reference frequency to the comparison frequency (step size), and an ‘N’ register that sets the division of the required synthesised frequency from the external VCO to the comparison frequency. This yields the required synthesised frequency (Fs), such that:

$Fs = (N/R) \times F_{REF}$ where F_{REF} is the selected reference frequency

Other parameters for the synthesisers are the charge pump setting (high or low).

Since the set-up for the PLLs takes four ‘RF Synthesiser Data register’ writes it follows that, while updating the PLL settings, the registers may contain unwanted or intermediate values of bits. These will persist until the last register is written. It is intended that users should change the content of the ‘RF Synthesiser Data register’ on a PLL that is disabled, powersaved or selected to work from the alternate register set (‘Tx’ and ‘Rx’ are alternate register sets). There are no interlocks to enforce this intention. The names ‘Tx’ and ‘Rx’ are arbitrary and may be assigned to other functions as required. They are independent sets of registers, one of which is selected to command each PLL by changing the settings in the RF Synthesiser Control - $B3 write register.

For optimum performance, a common master clock should be used for the RF synthesisers (the RF synthesiser clock) and the baseband sections (Main and Auxiliary System Clocks). Using unsynchronised clocks can result in spurious products being generated in the synthesiser output and in some cases difficulty may be experienced with obtaining lock in the RF synthesisers.

Lock Status

The lock status can be observed by reading the RF Synthesiser Status register, $B4, and the individual lock status bits can (subject to masking) provide a C-BUS interrupt.

The lock detector can use a tolerance of one cycle or four cycles of the reference clock (not the dividend version that is used as a comparison frequency) in order to judge phase lock. An internal shift register holds the last three lock status measurements and the lock status bits are flagged according to a majority vote of these previous three states. Hence one occasional lock error will not flag a lock fail. At least two successive phase lock events are required for the lock status to be true. Note that the lock status bits confirm phase lock to the measured tolerance and not frequency lock. The synthesiser may take more time to confirm phase lock with the lock status bits than the time to switch from channel to channel. The purpose of a four-cycle tolerance is for the case where a high frequency reference oscillator would not forgive a small phase error.

RF Inputs

The RF inputs are differential and self-biased (when not powersaved). They are intended to be capacitatively coupled to the RF signal. The signal should be in the range 0dBm to –20dBm (not necessarily balanced). To ensure an accurate input signal the RF should be terminated with 50Ω as close to the chip as possible and with the 'P' and 'N' inputs capacitatively coupled to the input and ground, keeping these connections as short as possible. The RF input impedance is almost purely capacitive and is dominated by package and printed circuit board parasitics.

Guidelines for using the RF Synthesisers

- RF input slew rate (dv/dt) should be 14V/µs minimum.
- The RF Synthesiser 2.5V digital supply can be powered from the VDEC output pin.
- RF clock sources and other, different clock sources must not share common IC components, as this may introduce coupling into the RF. Unused ac-coupled clock buffer circuits should be tied off to a dc supply, to prevent them oscillating.
- It is recommended that the RF Synthesisers are operated with maximum charge pump gain (i.e. ISET tied to RFVSS).
- The loop filter components should be optimised for each VCO.

6.14 Digital System Clock Generators

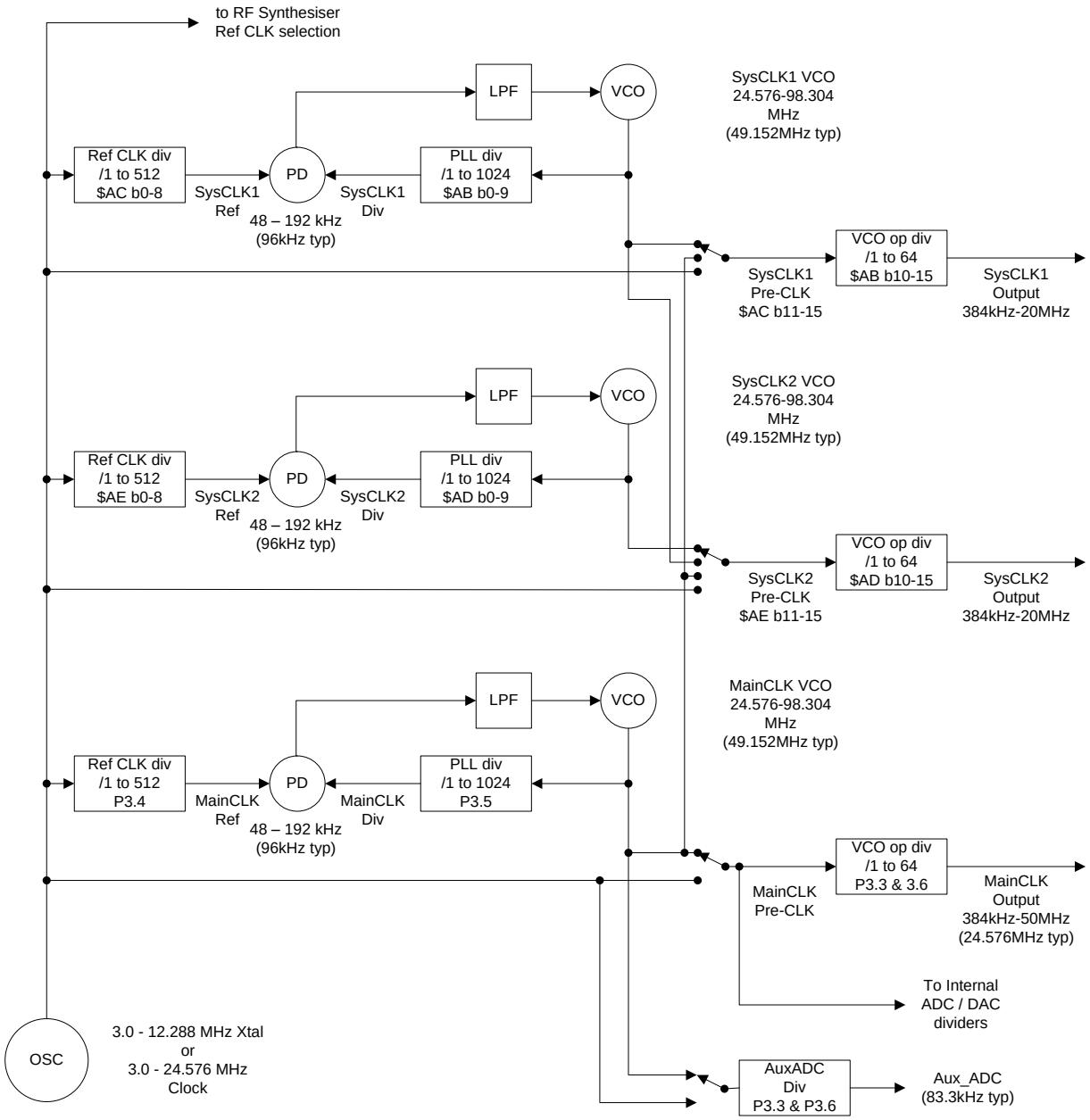


Figure 21 Digital Clock Generation Schemes

The CMX7131/CMX7141 includes a two-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in Section 4.2, or the XTAL input can be driven by an externally generated clock. The crystal (Xtal) source frequency can go up to 12.288MHz (clock source frequency up to 24.576MHz), but a 19.2MHz oscillator is assumed by default for the functionality provided in the CMX7131/CMX7141.

6.14.1 Main Clock Operation

A digital PLL is used to create the Main Clock (nominally 24.576MHz) for the internal sections of the CMX7131/CMX7141. At the same time, other internal clocks are generated by division of either the XTAL Reference Clock or the Main Clock. These internal clocks are used for determining the sample rates and conversion times of A-to-D and D-to-A converters, running a General Purpose (GP) Timer and the signal processing block. In particular, it should be noted that in Idle mode the setting of the GP Timer divider directly affects the C-BUS latency (with the default values this is nominally 250µs).

The CMX7131/CMX7141 defaults to the settings appropriate for a 19.2MHz oscillator, however if other frequencies are to be used then the Program Block registers P3.2 to P3.7 will need to be programmed appropriately at power-on. This flexibility allows the device to re-use an external clock source, so reducing total cost and potential noise sources. A table of common values is provided in Table 5.

See:

- Program Block 3 – AuxDAC, RAMDAC and Clock Control

6.14.2 System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. These are digital phase locked loop (PLL) clocks that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configure registers ($AB and $AD) control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configure registers ($AC and $AE) control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a reference frequency of 96kHz. If not required, these clocks can be independently powersaved. The clock generation scheme is shown in the block diagram of Figure 21.

See:

- SYSCLK 1 and SYSCLK 2 PLL Data - $AB, $AD write
- SYSCLK 1 and SYSCLK 2 REF - $AC and $AE write

NOTE: For minimum power consumption it is necessary to connect the SYSCLK1 and SYSCLK2 outputs to the PLL with the PLL powered down. **THIS IS NOT THE DEFAULT CONDITION**. To achieve minimum power write $8000 to registers $AC and $AE. With a 19.2MHz clock this will save around 1mA.

6.15 Signal Level Optimisation

The internal signal processing of the CMX7131/CMX7141 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) - (2 x 0.3V)] Volts pk-pk = 838mV rms, assuming a sine wave signal.

6.15.1 Transmit Path Levels

For the maximum signal out of the MOD1 and MOD2 attenuators, the signal level at the output of the Modem block is set to be 0dB, The Fine Output adjustment ($C3) has a maximum attenuation of 1.8dB and no gain, whereas the Coarse Output adjustment ($B0) has a variable attenuation of up to +40.0dB and no gain.

6.15.2 Receive Path Levels

In I/Q mode CMX7131/CMX7141 automatically manages the gain control settings to optimise signal levels. See also section 6.16.1.

6.16 CMX994 Operation

7131/7141FI-8.x is designed to work with the CMX994 Direct Conversion Receiver from CML by re-using the EEPROM serial interface. This requires that both BOOTEN1 and BOOTEN2 be pulled high (which is the same condition for loading the FI from the host over the C-BUS interface). Typical system performance using the CMX994 evaluation kit (EV9942) connected to the CMX7131/CMX7141 is shown in Table 14. Measurements use the EV9942 in default configuration with on-chip LNA; the LO is provided by an E4437B signal generator at 892MHz; received channel is 446.000MHz.

Table 14 Typical Performance with CMX994

Parameter	Measurement	Test Method
Sensitivity	-122 dBm	TIA-603-C (12 dB SINAD)
Adjacent Channel	69 dB	EN 300 086-1
Blocking	95 dB	EN 300 086-1
Intermodulation	67 dB	EN 300 086-1
Ultimate SINAD	47 dB	Standard input signal modulation at -80dBm.
CTCSS Squelch Opening	4 dB SINAD	TIA-603-C
CTCSS Audio Attach Time	225 ms	TIA-603-C
DCS Squelch Opening	8 dB SINAD	TIA-603-C
DCS Audio Attach Time	295 ms	TIA-603-C

6.16.1 Signal Level

In order for the 7131/7141FI-8.x internal processing to work correctly the gain through the RF path must be close to nominal value. To confirm that the RF and interface design is correct apply a signal to the input of the receiver at a level of -65dBm. (Note: the signal should have a small frequency offset from the nominal channel centre). The resulting signal at the DISCFB and ALTFB pins should be a sine wave of approximately 510mVp-p.

6.16.2 Powersave

The powersave features of the 7131/7141FI-8.x can be used to reduce the average power consumption of the CMX994. Details of the powersave modes are given in section 6.8.9. On entering powersave the CMX994 receiver sections are automatically powered-down by C-BUS commands. It is recommended that the RXEN and TXEN pins on the CMX994 are also held low. (Note: if the CMX994 PLL is being used it is not powersaved).

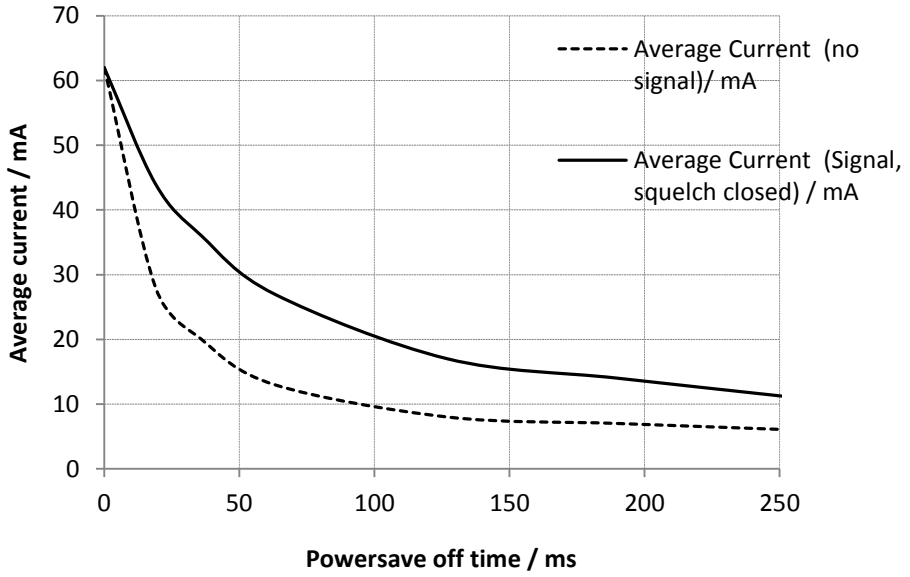


Figure 22 CMX994 Powersaving as a Function of Sleep Period

The level of powersaving achieved depends on the length of the powersave off time (programmable using register $CD) and also depends on the state of the RF channel. Figure 22 shows two curves, one with no signal present and the other with a signal present but one that does not open the squelch. The first state achieves lower power because the CMX7131/CMX7141 can return to the powersave condition earlier, as it does not have to continue processing to evaluate the squelch threshold. The current shown in Figure 22 is for the complete CMX994 receiver but does not include the power taken by local oscillator circuits.

6.16.3 Powersave Thresholds

Powersave thresholds are described in section 6.8.9. With the default settings the powersave will reliably trigger with a signal at -122dBm (typical level for 12dB SINAD). With no signal applied the threshold will occasionally trigger. Adjusting the threshold levels can avoid false triggering but at the expense of the reliability of triggering at minimum SINAD. The default powersave off time is 25ms.

6.16.4 RSSI

A measure of the received signal strength (RSSI) is provided in the Aux 1 Data and Status register ($A9). Typical performance with the CMX994 is shown in Figure 23.

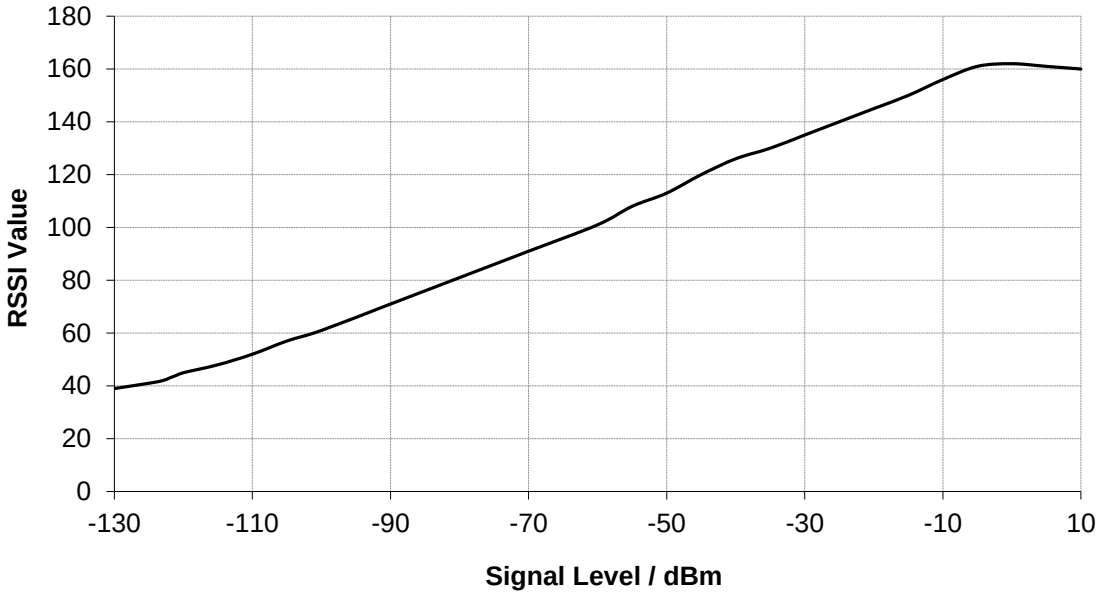


Figure 23 RSSI Value vs. CMX994 Input Level

6.16.5 Frequency Error

A measure of the frequency error of the received signal is provided in the Aux 1 Data and Status register ($A9). The measurement is a 2's complement number valid over the range ±2kHz; outside that range the measurement will fold back. Typical performance is shown in Figure 24.

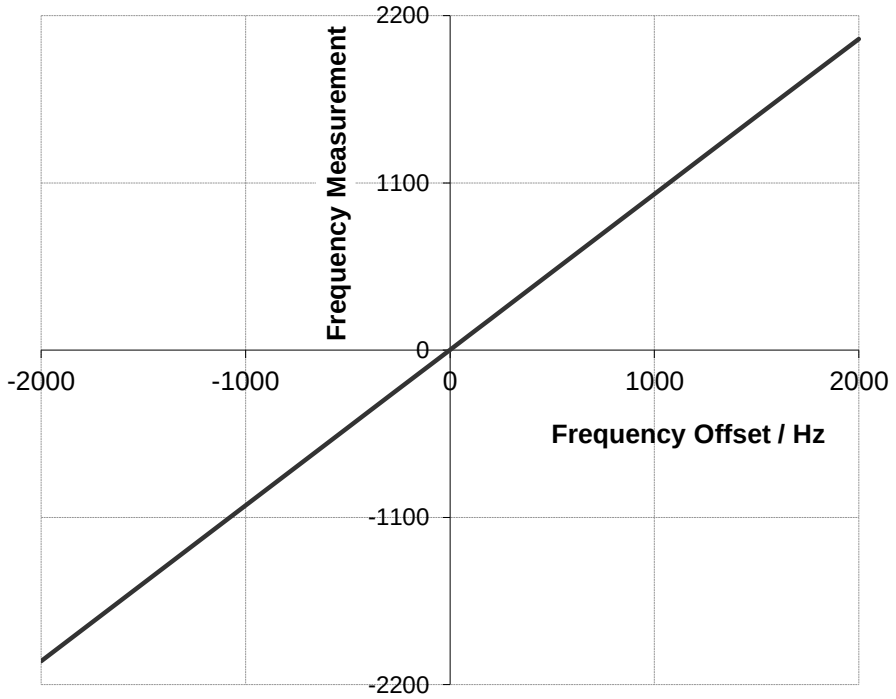


Figure 24 Frequency Error Measurement

6.17 C-BUS Register Summary

Table 15 C-BUS Registers

ADDR. (hex)	R/W	REGISTER	Word Size (bits)
$01	W	C-BUS RESET	0
$A7	W	AuxADC Configuration	16
$A8	W	AuxDAC Data and Control	16
$A9	R	Aux 1 Data and Status/Checksum 2 hi	16
$AA	R	Aux 2 Data and Status/Checksum 2 lo	16
$AB	W	SYSCLK 1 PLL Data	16
$AC	W	SYSCLK 1 Ref	16
$AD	W	SYSCLK 2 PLL Data	16
$AE	W	SYSCLK 2 Ref	16
$AF		*Reserved*	
$B0	W	Analogue Output Gain	16
$B1	W	Input Gain and Signal Routing	16
$B2	W	RF Synthesiser Data (CMX7131 only)	16
$B3	W	RF Synthesiser Control (CMX7131 only)	16
$B4	R	RF Synthesiser Status (CMX7131 only)	8
$B5	W	TxData0	16
$B6	W	TxData1	16
$B7	W	TxData2	16
$B8	R	RxData0/Checksum 1 hi	16
$B9	R	RxData1/Checksum 1 lo	16
$BA	R	RxData2	16
$BB	R	RxData3	16
$BC		*Reserved*	
$BD		*Reserved*	
$BE		*Reserved*	
$BF		*Reserved*	
$C0	W	Power Down Control	16
$C1	W	Mode Control	16
$C2	W	Analogue Mode	16
$C3	W	Analogue Level	16
$C4		*Reserved*	
$C5	R	RxData4	16
$C6	R	IRQ Status	16
$C7	W	Modem Configuration	16
$C8	W	Programming Register	16
$C9	R	Modem Status	16
$CA	W	TxData3	16
$CB	W	TxData4	16
$CC	R	Analogue Status	16
$CD	W	Aux Config	16
$CE	W	Interrupt Mask	16
$CF		*Reserved*	

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

7 Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD}- DV_{SS}	–0.3	4.5	V
AV_{DD}- AV_{SS}	–0.3	4.5	V
RFV_{DD}- RFV_{SS} (CMX7131 only)	–0.3	4.5	V
CPV_{DD}- RFV_{SS} (CMX7131 only)	–0.3	4.5	V
Voltage on any pin to DV_{SS}	–0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	–0.3	AV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding BIAS) (i.e. VDEC, AVDD, AVSS, DVDD, DVSS, CPVDD, RFVDD or RFVSS)	–30	+30	mA
Current into or out of any other pin	–20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD} or CPV_{DD}	0	0.3	V
AV_{DD} and CPV_{DD} (CMX7131 only)	0	0.3	V
DV_{SS} and AV_{SS} or RFV_{SS} (CMX7131 only)	0	50	mV
AV_{SS} and RFV_{SS} (CMX7131 only)	0	50	mV

L4 Package (48-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1600	mW
... Derating	–	16	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

L9 Package (64-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1690	mW
… Derating	–	16.9	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q1 Package (64-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	3500	mW
… Derating	–	35.0	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
$DV_{DD} – DV_{SS}$		3.0	3.6	V
$AV_{DD} – AV_{SS}$		3.0	3.6	V
$CPV_{DD} – RFV_{SS}$ (CMX7131 only)		3.0	3.6	V
$RFV_{DD} – DV_{SS}$ (CMX7131 only)	3	2.25	2.75	V
$V_{DEC} – DV_{SS}$	2	2.25	2.75	V
Operating Temperature		−40	+85	°C
XTAL/CLK Frequency (using an Xtal)	1	3.0	12.288	MHz
XTAL/CLK Frequency (using an external clock)	1	3.0	24.576	MHz

Notes:
1 Nominal XTAL/CLK frequency is 19.2MHz.
2 The V_{DEC} supply is automatically derived from DV_{DD} by the on-chip voltage regulator.
3 The RFV_{DD} supply can be supplied from the V_{DEC} supply, if preferred.

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2. Maximum load on digital outputs = 30pF.
Oscillator Frequency = 19.2MHz ±0.01% (100ppm); T_{AMB} = –40°C to +85°C.
AV_{DD} = DV_{DD} = CPV_{DD} (CMX7131) = 3.0V to 3.6V; RFV_{DD} (CMX7131) = 2.25V to 2.75V.
V_{DEC} = 2.5V.

Current consumption figures quoted in this section apply to the device when loaded with 7131/7141FI-8.x only. The use of other CMX7131/CMX7141 Function Images, will modify the current consumption of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
DI_{DD}		–	8	100	µA
AI_{DD}		–	4	20	µA
Idle Mode	22				
DI_{DD}		–	1.4	–	mA
AI_{DD}	23	–	1.6	–	mA
Rx Mode	22				
DI_{DD} (Voice+ de-emphasis)		–	8.3	–	mA
DI_{DD} (During powersave cycle)		–	3.3	–	mA
AI_{DD} (Voice+ de-emphasis)		–	5.0	–	mA
AI_{DD} (During powersave cycle)		–	3.0	–	mA
Tx Mode	22				
DI_{DD} (Voice+pre-emphasis – two-point)	22a	–	8.0	–	mA
DI_{DD} (Voice+preemphasis – I/Q)		–	8.1	–	mA
AI_{DD} (Voice+pre-emphasis – two-point)	22a	–	3.6	–	mA
AI_{DD} (Voice+preemphasis – I/Q)		–	4.7	–	mA
Additional Current for each Auxiliary System Clock (output running at 4MHz)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	250	–	µA
Additional Current for each Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	50	–	µA
Additional Current for each Auxiliary DAC					
AI_{DD} (AV_{DD} = 3.3V)		–	200	–	µA
Additional Current for each RF Synthesiser	24				
CPI_{DD} + RFI_{DD} (CPV_{DD} = 3.3V, RFV_{DD} = 2.5V)		–	2.5	4.5	mA

Notes:

21 T_{AMB} = 25°C: not including any current drawn from the device pins by external circuitry.

22 System Clocks: auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled.

22a OP1 enabled, OP2 disabled.

23 May be further reduced by power-saving unused sections

24 When using the external components shown in Figure 19 and when supplying the current for RFV_{DD} from the regulated 2.5V digital (V_{DEC}) supply. The latter is derived from DV_{DD} by an on-chip voltage regulator.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input	25				
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		−40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Leakage Current (Logic 1 or 0)		−1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic 1 (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic 0 (I_{OL} = -5mA)		–	–	10%	DV_{DD}
'Off' State Leakage Current		–	–	10	µA
IRQN (Vout = DV_{DD})		−1.0	–	+1.0	µA
REPLY_DATA (output HiZ)		−1.0	–	+1.0	µA
V_{BIAS}	26				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	22	–	kΩ

Notes: 25 Characteristics when driving the XTAL/CLK pin with an external clock source.

26 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' Pulse Width		31	15	–	–	ns
'Low' Pulse Width		31	15	–	–	ns
Input Impedance (at 6.144MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)			–	20	–	ms
System Clk 1/2 Outputs						
XTAL/CLK input to CLOCK_OUT timing:						
(in high to out high)		32	–	15	–	ns
(in low to out low)		32	–	15	–	ns
'High' Pulse Width		33	76	81.38	87	ns
'Low' Pulse Width		33	76	81.38	87	ns
V_{BIAS}						
Start-up Time (from powersave)			–	30	–	ms
Microphone, Alternative and Discriminator Inputs (MIC, ALT, DISC)						
Input Impedance		34	–	>10	–	MΩ
Maximum Input Level (pk-pk)		35	–	–	80%	AV_{DD}
Load Resistance (feedback pins)			80	–	–	kΩ
Amplifier Open Loop Voltage Gain (I/P = 1mVrms at 100Hz)			–	80	–	dB
Unity Gain Bandwidth			–	1.0	–	MHz
Programmable Input Gain Stage		36				
Gain (at 0dB)		37	−0.5	0	+0.5	dB
Cumulative Gain Error (wrt attenuation at 0dB)		37	−1.0	0	+1.0	dB

Notes:

31 Timing for an external input to the XTAL/CLK pin.

32 XTAL/CLK input driven by an external source.

33 6.144MHz XTAL fitted and 6.144MHz output selected (scale for 19.2MHz).

34 With no external components connected, measured at DC.

35 Centred about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

36 Gain applied to signal at output of buffer amplifier: DISCFB, ALTFB or MICFB.

37 Design Value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1/2 and Audio Output (MOD 1, MOD 2, AUDIO)					
Power-up to Output Stable	41	–	50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)	43	–1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		–0.6	0	+0.6	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ
Audio Attenuator					
Attenuation (at 0dB)	43	–1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		–1.0	0	+1.0	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

42 Small signal impedance, at AV_{DD} = 3.3V and T_{AMB} = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centred about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (Aux ADC 1 to 4)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10-bit ADCs					
Resolution		–	10	–	Bits
Maximum Input Level (pk-pk)	54	–	–	80%	AV_{DD}
Conversion Time	52	–	250	–	µs
Input Impedance					
Resistance	57	–	>10	–	MΩ
Capacitance		–	5	–	pF
Zero Error	55	0	–	±10	mV
Integral Non-linearity		–	–	±3	LSBs
Differential Non-linearity	53	–	–	±1	LSBs
Auxiliary 10-bit DACs					
Resolution		–	10	–	Bits
Maximum Output Level (pk-pk), no load	54	80%	–	–	AV_{DD}
Zero Error	56	0	–	±10	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity		–	–	±4	LSBs
Differential Non-linearity	53	–	–	±1	LSBs

Notes:

51 Denotes output impedance of the driver of the auxiliary input signal, to ensure <1 bit additional error under nominal conditions.

52 With an auxiliary clock frequency of 6.144MHz.

53 Guaranteed monotonic with no missing codes.

54 Centred about $AV_{DD}/2$.

55 Input offset from a nominal V_{BIAS} input, which produces a $0200 ADC output.

56 Output offset from a $0200 DAC input, measured with respect to nominal V_{BIAS} output.

57 Measured at dc.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
RF Synthesisers – Phase Locked Loops					
Reference Clock Input					
Input Logic 1	62	70%	–	–	RFV_{DD}
Input Logic 0	62	–	–	30%	RFV_{DD}
Frequency	64, 66	5.0	19.2	40.0	MHz
Divide Ratios (R)	63	2	–	8191	
Each RF Synthesiser	69				
Comparison Frequency		–	–	500	kHz
Input Frequency Range	67	100	–	600	MHz
Input Level		−15	–	0	dBm
Input Slew Rate		14	–	–	V/µs
Divide Ratios (N)		1088	–	1048575	
1Hz Normalised Phase Noise Floor	68	–	−197	–	dBc/Hz
Charge Pump Current (I_{CP}) (high)	65	±1.88	±2.5	±3.3	mA
Charge Pump Current (I_{CP}) (low)	65	±470	±625	±820	µA
Charge Pump Current – voltage variation		–	10%	–	per V
Charge Pump Current – sink-to-source match		–	5%	–	of I_{CP}

Notes:

62 Square wave input.

63 Separate dividers are provided for each PLL.

64 For optimum performance of the synthesiser subsystems, a common master clock should be used for the RF Synthesisers and the baseband sections. Using unsynchronised clocks is likely to result in spurious products being generated in the synthesiser outputs and in some cases difficulty may be experienced in obtaining lock in the RF Synthesisers.

65 External ISET resistor (R31) = 0Ω (Internal ISET resistor = 9k6Ω nominally).

66 Lower input frequencies may be used subject to division ratio requirements being maintained.

67 Operation outside these frequency limits is possible, but not guaranteed. Below 150MHz, a square wave input may be required to provide a fast enough slew rate.

68 1Hz Normalised Phase Noise Floor (PN1Hz) can be used to calculate the phase noise within the PLL loop by:
Phase Noise (in-band) = $PN1Hz + 20\log_{10}(N) + 10\log_{10}(f_{comparison})$.

69 It is recommended that RF Synthesiser 1 be used for the higher frequency use (e.g. RF 1st LO) and RF Synthesiser 2 be used for lower frequency use (e.g. IF LO).

7.1.4 Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in Figure 2 / Figure 6.
Maximum load on digital outputs = 30pF.
Oscillator Frequency = 19.2MHz ±0.01% (100ppm); T_{AMB} = −40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.

All figures quoted in this section apply to the device when loaded with FI-8.0.x connected to a CMX994 only.

I/Q Performance	Notes	Min.	Typ.	Max.	Unit
Rx Sensitivity (12dB SINAD)	74,75	–	-122	–	dBm
Rx Adjacent Channel Rejection	74,75		47.5	–	dB
Rx Adjacent Channel Rejection	75,76	–	69		dB
Rx Alternate Channel Rejection	75,76		71		dB
Rx Blocking	74,75		95		dB
Rx Intermodulation	75,76	–	67		dB

Audio Performance	Notes	Min.	Typ.	Max.	Unit
Audio Compandor					
Attack Time		–	4.0	–	ms
Decay Time		–	13	–	ms
0dB-point	85	–	N/A	–	mVrms
Compression/Expansion Ratio		–	2:1	–	
Audio Tone Generator					
Frequency Range		288	–	3000	Hz
Tone Frequency Accuracy		–	–	±0.3	%
Tone Amplitude Tolerance		−1.0	0	+1.0	dB
Total Harmonic Distortion	80	–	2.0	4.0	%
Analogue Channel Audio Filtering					
Pass-band (nominal bandwidth):					
12.5kHz Channel	83	300	–	2550	Hz
25kHz Channel	83	300	–	3000	Hz
Pass-band Gain (at 1.0kHz)		–	0	–	dB
Pass-band Ripple (wrt gain at 1.0kHz)		−2.0	0	+0.5	dB
Stop-band Attenuation		33.0	–	–	dB
Residual Hum and Noise Tx	86	–	-66	–	dB
Residual Hum and Noise Rx (with CTCSS)	75, 84	–	46	–	dB
Residual Hum and Noise Rx (with DCS)	75, 84	–	44	–	dB
Pre-emphasis	83	–	+6	–	dB/oct
De-emphasis	83	–	−6	–	dB/oct
Audio Scrambler					
Inversion Frequency		–	3300	–	Hz
Pass-band		320	–	2900	Hz
Audio Expandor					
Input Signal Range	85	–	–	N/A	Vrms

CTCSS Detector						
SINAD Opening		71, 74	–	4	–	dB
Sensitivity		74	–	−124	–	dBm
Response Time	(Composite Signal)	73	–	225	250	ms
De-response Time	(Composite Signal)	73	–	210	250	ms
Dropout Immunity		73	–	160	–	ms
Falsing		73	–	1	–	
Frequency Range			60	–	260	Hz
Tone Frequency Accuracy			–	–	±0.3	%
Tone Amplitude Tolerance			−1.0	0	+1.0	dB
Total Harmonic Distortion			–	2.0	4.0	%
DCS Decoder						
SINAD Opening		71				dB
Sensitivity		71	–	–	–	
Response Time	(Composite Signal)	71	–	295	–	ms
Bit-Rate Sync Time			–	2	–	edges
Bit Rate			–	134.4	–	bps
Amplitude Tolerance			−1.0	0	+1.0	dB

FFSK Modem	**Notes**	**Min.**	**Typ.**	**Max.**	**Unit**
Modem Symbol Rate		–	1200	–	symbols /s
Logic 1 frequency		1198	1200	1202	Hz
Logic 0 frequency		1798	1800	1802	Hz
Isochronous Distortion (0 to 1 and 1 to 0)		–	–	40	µs
3rd Harmonic Distortion		–	–	3	%
Rx Co-channel Rejection	70, 72	15	12	–	dB
Bit Error Rate (SNR = 20dB)	73	–	<1	–	10^{-8}
Probability of bit 16 being correct		–	>99.9	–	%

Notes:

70 Transmitting continuous default preamble.
71 See section 6.16.
72 For a 12.5 kHz channel.
73 Combined performance of CMX7131/CMX7141 and CMX994 connected as shown in Figure 6 using EV9942 and PE0201; measurement method from EN 301 166.
74 Test Method TIA-603-C.
75 For a 12.5kHz channel; Combined performance of CMX7131/CMX7141 and CMX994 connected as shown in Figure 6 using EV9942 and PE0201.
76 Test Method EN 300 086.

80 Measured at MOD 1 or MOD 2 output.
81 Void
82 Void
83 See Figure 12 and Figure 13.
84 Test method TIA-603-C section 2.4.5; CTCSS: 254 Hz tone (worst case), DCS: Octal Code 532.
85 Internal signal.
86 Tx (two-point) hum and noise is wrt 308mV rms and with the following analogue processing: scrambler, pre-emphasis, 300Hz high-pass filter, channel filter.

7.2 C-BUS Timing

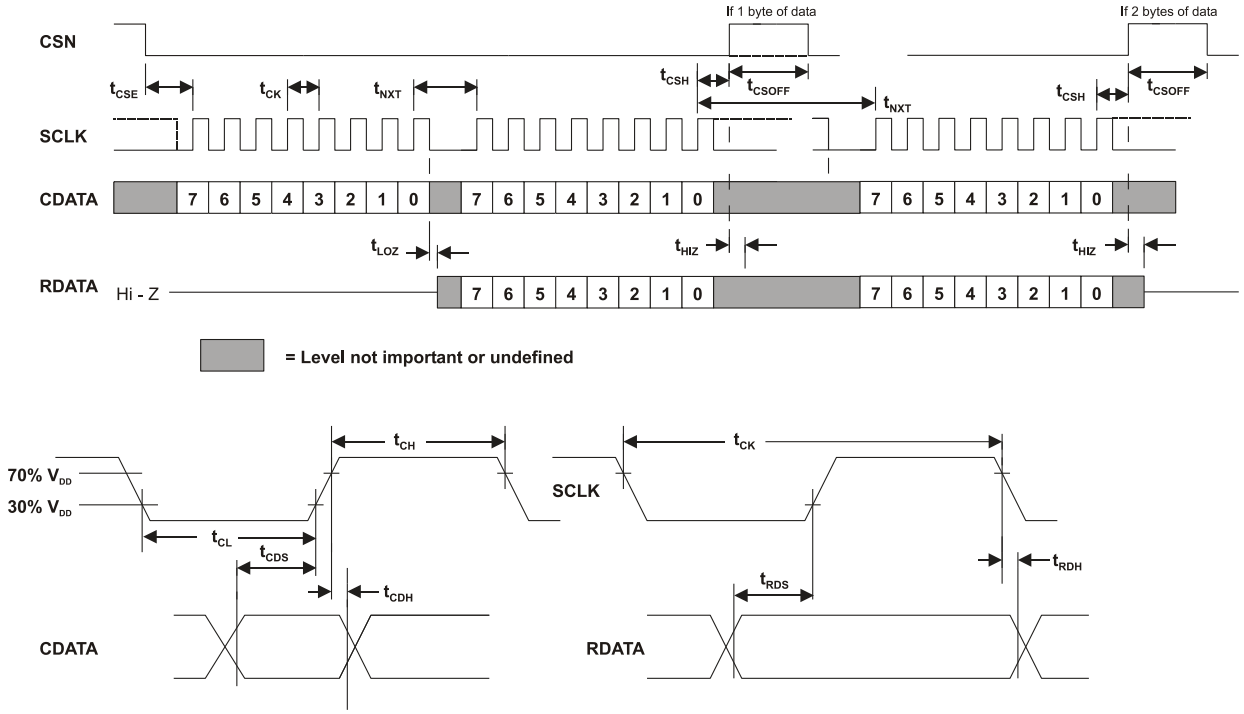


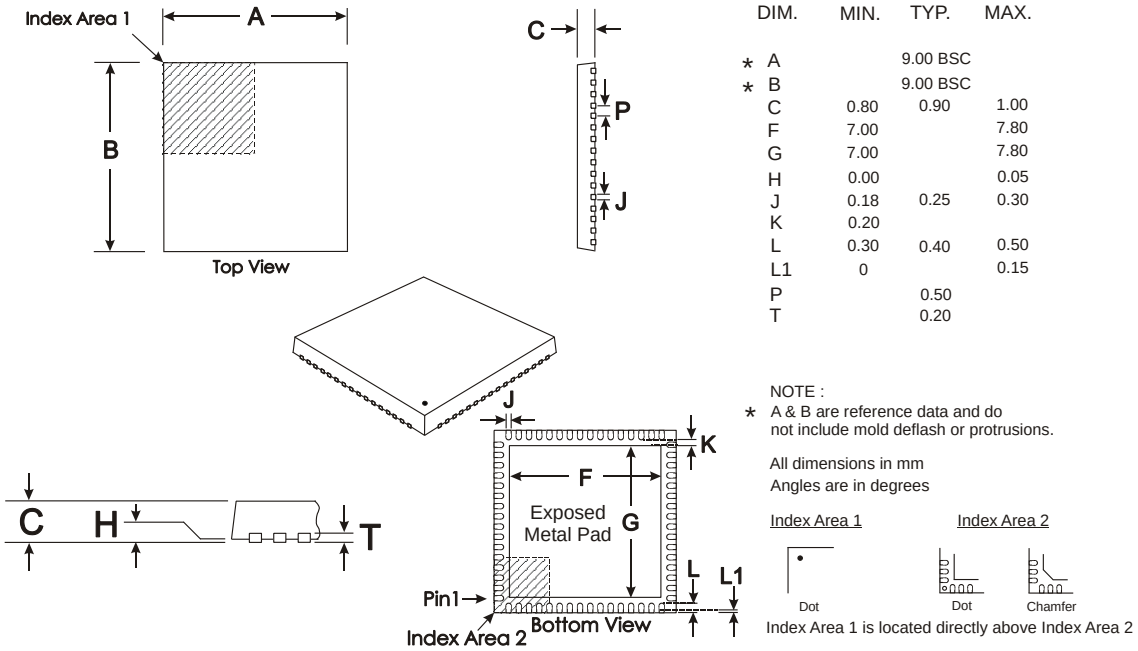
Figure 25 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA Output Enable Time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	SCLK cycle time		200	–	–	ns
t_{CH}	SCLK high time		100	–	–	ns
t_{CL}	SCLK low time		100	–	–	ns
t_{CDS}	CDATA setup time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA setup time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes:
1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7131/CMX7141 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

7.3 Packaging.



	DIM.	MIN.	TYP.	MAX.
*	A		9.00 BSC	
*	B		9.00 BSC	
	C	0.80	0.90	1.00
	F	7.00		7.80
	G	7.00		7.80
	H	0.00		0.05
	J	0.18	0.25	0.30
	K	0.20		
	L	0.30	0.40	0.50
	L1	0		0.15
	P		0.50	
	T		0.20	

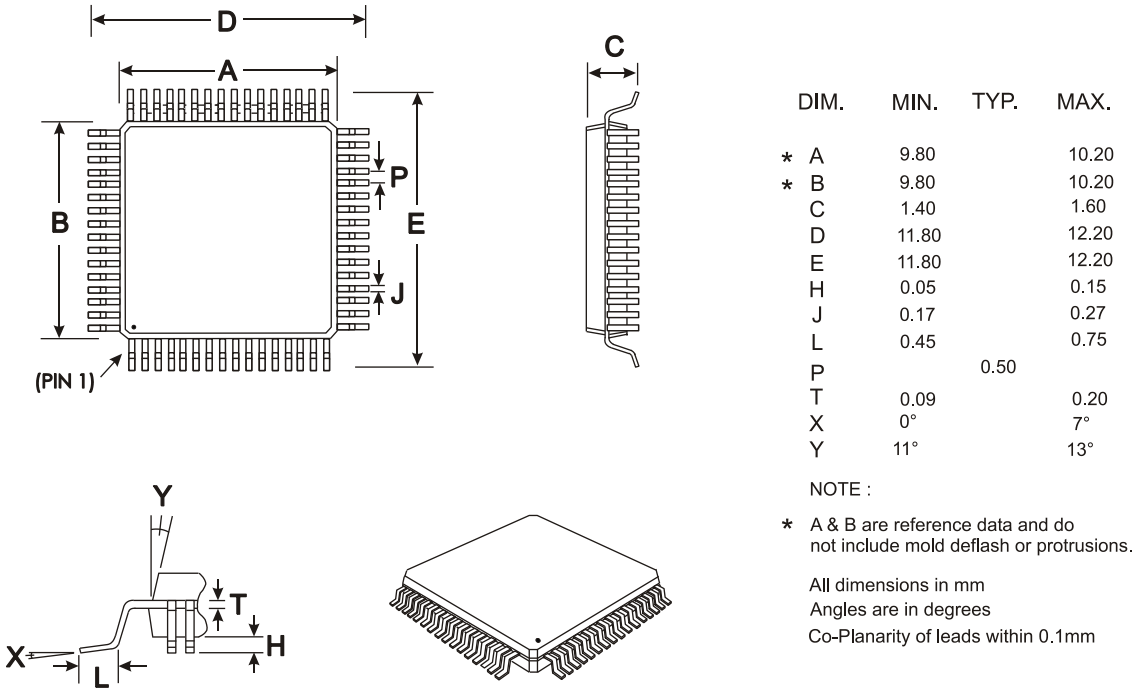
NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 26 Mechanical Outline of 64-pin VQFN (Q1)

Order as part no. CMX7131Q1



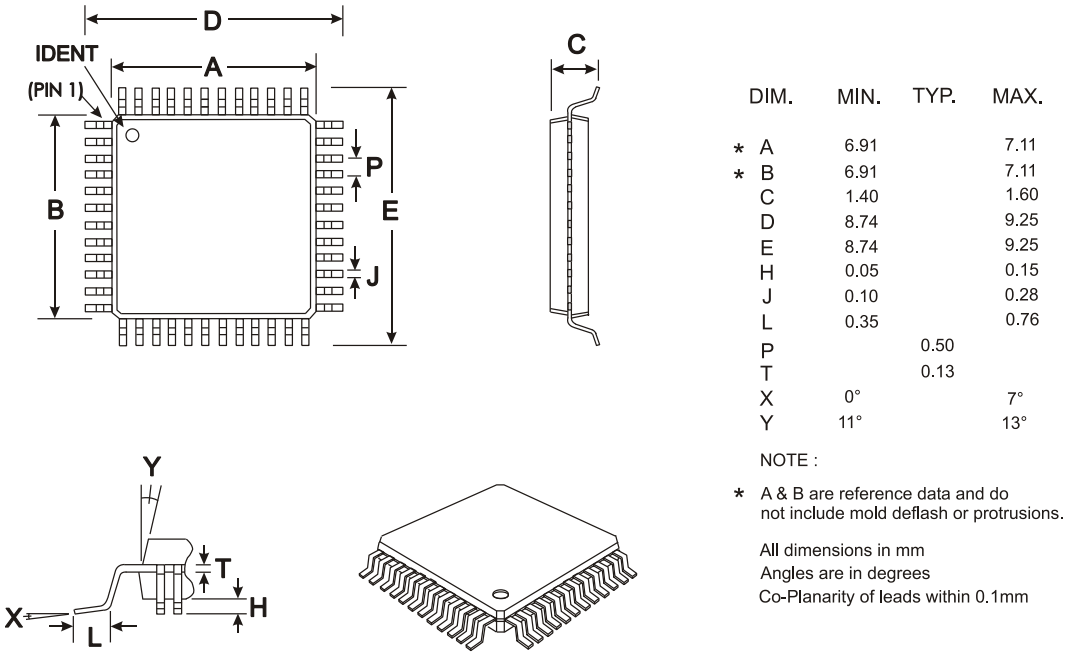
	DIM.	MIN.	TYP.	MAX.
*	A	9.80		10.20
*	B	9.80		10.20
	C	1.40		1.60
	D	11.80		12.20
	E	11.80		12.20
	H	0.05		0.15
	J	0.17		0.27
	L	0.45		0.75
	P		0.50	
	T	0.09		0.20
	X	0°		7°
	Y	11°		13°

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 27 Mechanical Outline of 64-pin LQFP (L9)

Order as part no. CMX7131L9



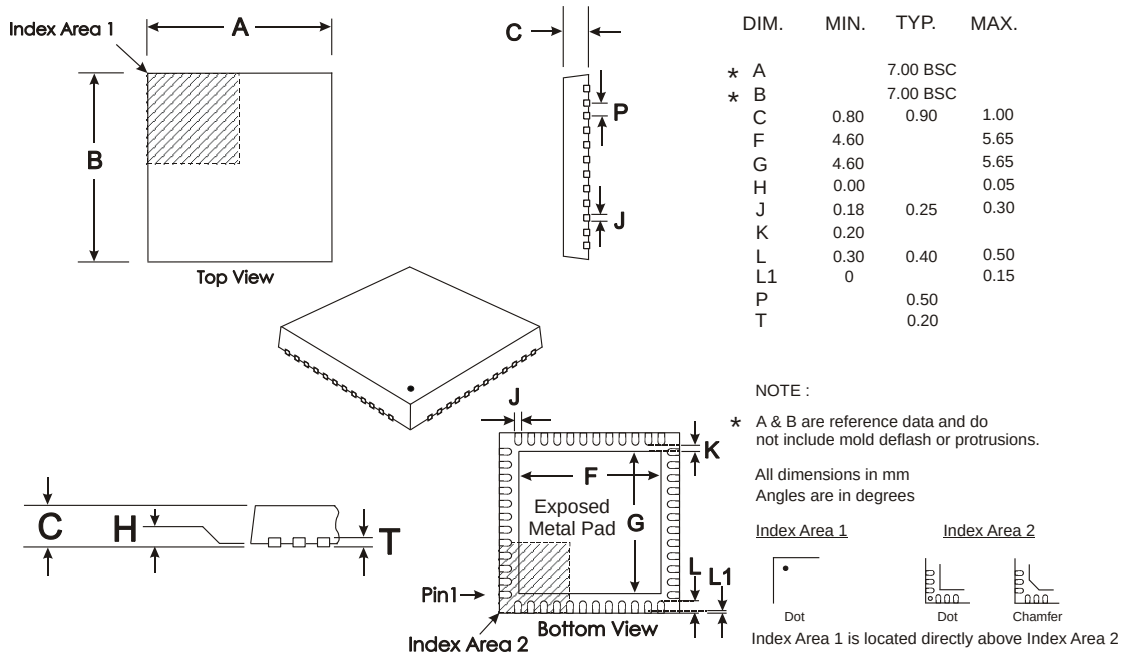
DIM.	MIN.	TYP.	MAX.
* A	6.91		7.11
* B	6.91		7.11
C	1.40		1.60
D	8.74		9.25
E	8.74		9.25
H	0.05		0.15
J	0.10		0.28
L	0.35		0.76
P		0.50	
T		0.13	
X	0°		7°
Y	11°		13°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 28 Mechanical Outline of 48-pin LQFP (L4)
Order as part no. CMX7141L4



DIM.	MIN.	TYP.	MAX.
* A		7.00 BSC	
* B		7.00 BSC	
C	0.80	0.90	1.00
F	4.60		5.65
G	4.60		5.65
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 Index Area 2

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 29 Mechanical Outline of 48-pin VQFN (Q3)
Order as part no. CMX7141Q3

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Design Support/Package Information page of the CML website: [www.cmlmicro.com].

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